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AN ANALYSIS OF HF RADIO AND ERROR CORRECTION CODING IN THE CONUS AUTODIN SYSTEM

Donald G. Iram

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Air Force Systems Command
Griffiss Air Force Base, New York

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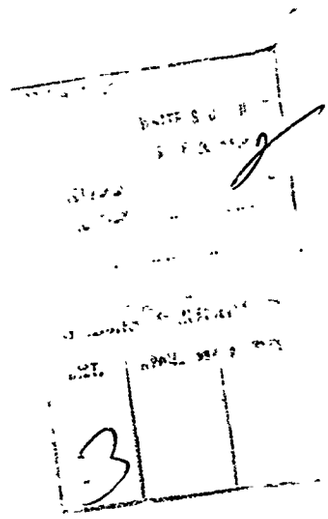

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AN ANALYSIS OF HF RADIO AND ERROR CORRECTION CODING IN THE CONUS AUTODIN SYSTEM

Donald G. Iram

AFLC, GAFB, N.Y., 20 Mar 68-51

FOREWORD

The goals of this project could not have been attained without the services and facilities provided by the Army, the Navy, the Air Force Communications Service and the Defense Communications Agency.

Outstanding individual efforts by personnel assigned to this program were too numerous to mention in this brief foreword. The author would be remiss, however, if he did not acknowledge the efforts of Mr. Evan Pike of the 2049th Communications Group, McClellan AFB; Mr. A. W. Barany of the U. S. Naval Communications Unit, Hancock Field; and Lt E. H. Knudsen of the Naval Communications System Headquarters, Baileys Crossroads, Va. These men made it possible for us to introduce our experimental program into the dynamic environment of the AUTODIN switches and the operational radio sites on the west coast.

For their constant attention to all details of this program and for their willingness to devote long hours to the author's many problems, I would like to thank my mentors: Mr. Harold Crowley of RADC and Mr. Arthur Bugg of DCA.

This technical report has been reviewed and is approved.

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ABSTRACT

The Defense Communications Agency (DCA) sought to determine if the quality of high speed digital data transmitted over long-haul HF radio circuits could be improved by the use of commercially available forward error correction (FEC) devices. The DCA objective was to improve the bit error rate such that HF radio channels could be reliably used as overflow and restoral circuits between Switching Centers within the AUTODIN System. Accordingly, a study, analysis, and test program was initiated at RADC to satisfy the following requirements defined by DCA:

- To determine the maximum data rate transmission over HF radio channels within allowable AUTODIN error rates using FEC devices.
- To determine the actual extent of improvement through the use of FEC devices.
- To analyze FEC operation within the AUTODIN ARQ System.
- To ascertain modifications for efficient operation of:
  - AUTODIN ARQ
  - AUTODIN Procedures
  - AUTODIN Modems
- To provide a procurement specification for DCA use in future equipment purchases.

The study portion of the program resulted in recommendations for the procurement of three representative, commercially available coding equipments and for a fully documented test plan for the evaluation of these equipments on a transcontinental HF radio circuit.

A three-phase test program was carried out during the months of February through August 1967. A full duplex HF radio path was established between McClellan AFB in Sacramento, California, and Griffiss AFB, Rome, New York. The AUTODIN Switches at McClellan AFB and at Hancock Field, Syracuse, New York, were connected to the radio path by data quality phone lines and microwave links. In one of the test phases, AUTODIN traffic was passed between these two terminals in full duplex operation for a period of five weeks. Circuit quality was evaluated in terms of block error rate and data throughput rate for uncoded data and for data protected by each of the FEC devices tested. The other two test phases were concerned with deriving the fine grain

bit error pattern statistics of the channel and an analysis of the operation of the AUTODIN data switches. The latter test phase utilized the DICOSE facility at RADC to simulate AUTODIN switch operation in order to obtain data that was not available in normal AUTODIN switch operation.

Over 375 hours of data taken at trunk data rates of 1200 bits per second were analyzed. Performance characteristics for each of the error correction devices tested as well as the uncoded channel operation were provided to DCA. A recommendation incorporating an error correction device into the AUTODIN System for use on HF radio backup circuits was made. The recommendation included a complete procurement specification. In addition, recommendations were made concerning modem operation and the interface of the AUTODIN switch with the HF radio sites.

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INTRODUCTION

The Defense Communications Agency (DCA) sought to determine if the quality of high speed digital data transmitted over long haul HF radio circuits could be improved by the use of commercially available forward error correction devices. The DCA objective was to improve the bit error rate such that HF radio channels could be reliably used as overflow and restoral trunk circuits between Automatic Switching Centers within the AUTODIN System.

The problem is two-fold. An error correction technique was needed that would provide a significant improvement in the error rate experienced on these circuits. The error-correction devices used had to interface with the AUTODIN System without causing degradation in the operating efficiency of the AUTODIN Switching Centers.

The data source, data sink, data rate and data format were all fixed. All of the terminal equipment, including crypto devices and the data modem, were fixed for the purposes of this program. The foremost problem was the AUTODIN system constraint and its effect on the time available for the data encoding and decoding processes.

AUTODIN Time Constraint (1) (2)

Messages transmitted on trunk circuits between AUTODIN Switching Centers consist of one or more data blocks. Each data block consists of 84, eight-bit data characters. The first character in the block is always a framing character. The second character will be a Language Media Format (LMF) Indicator or will identify the security classification of the block.

The first block in the message will have an LMF character and will indicate to the receive terminal the output device (Teletypewriter format, magnetic tape, card format etc.) associated with the message. The next 80 characters will be data characters. The 83rd character will be a frame character indicating either the end of the block or, if it is the last block in the message, the end of the text. The 84th and last character will always be a block parity check character. Each character contains 7 information bits in positions 1 through 7. The eighth bit in every character is always a lateral parity check bit on the character. The block parity character is formed by a longitudinal parity check across the characters in the block, i.e. bit position 1 of the block parity character is a parity check on bit position one of every character in the block except the first character. The message frame character is not included in the block parity check. Bit positions 2 through 8 of the block parity character are formed in a similar manner. The receive terminal checks the lateral parity bits and the block parity check character of each received block. If all the parity checks are correct, the receive terminal will transmit an acknowledgement

(ACK) character back to the transmit terminal. If any parity is incorrect, the receive terminal will initiate a message repeat (NACK) character.

The transmit terminal, when operating in the continuous block mode, will transmit a message block immediately followed by a second message block. The block framing character of the second block is transmitted contiguous with the block parity character of the first block. An answer timer is set when the end of block framing character of the first block is transmitted.

The ACK or NACK character must be received from the receive terminal prior to the transmission of the 83rd character of the second block. If an ACK or NACK character is not received in this period, continuous transmission stops. The 83rd character of the second block is not sent. Instead, a reply (REP) character is transmitted, directing the receiver to send its answer to the last block transmitted. The answer timer is reset when the REP character is transmitted. If an answer is not received, and the answer timer expires, the REP sequence is reinitiated. After three REP characters are sent and still no answer is received, an alarm is triggered. Typical answer timer settings used in CONUS AUTODIN are 250 to 500 milliseconds for 1200 and 2400 baud circuits.

Two acknowledgment characters are used, identified as ACK-1 and ACK-2, to maintain block synchronization. As soon as the transmit terminal receives an ACK-1 character from the receive terminal, a third line block is loaded into the buffer that contained line block 1. The transmit terminal will then expect an ACK-2 character to acknowledge the line block stored in the second buffer. In the absence of a NACK character, the transmit terminal will expect to receive alternating ACK-1 and ACK-2 characters, corresponding to line blocks unloaded from the first and the second block buffer store.

A successful block transmission requires that 672 successive bits (84 characters 8 bit per character) be received error free. In addition, the acknowledgment characters must be received error free at the transmitter. Failure to meet these conditions will cause a re-transmission.

On long haul HF radio circuits with data transmitted at trunk bit rates, the line-block retransmission rate may be sufficiently high so as to make this medium inefficient for AUTODIN trunk traffic.

The DCA felt that this situation might be improved by use of forward error correction coding devices. They desired to investigate the possibility that commercially available coding equipment existed that could be used "in between" the AUTODIN error detection code to significantly improve the information throughput rate on HF radio circuits. They therefore requested the Air Force to evaluate the ability of commercially available forward error correction equipment to significantly improve the AUTODIN information throughput rate for trunk operation on HF radio. They stipulated that any equipments used had to operate without any modification to the existing AUTODIN

system. This task was assigned by Headquarters USAF to the Rome Air Development Center (RADC).

To maintain continuous data transmission on AUTODIN trunk circuits, the transmit terminal must receive an ACK character for a transmitted block prior to the transmission of the 83rd character of the following block. This allows approximately 656 bit times for coding, transmission, decoding and AUTODIN processing. Since the circuit is full-duplex, the acknowledgment characters will encounter the same delays in the return path.

Western Union, at the request of DCA, performed a study [3] of the delay times involved in the AUTODIN processing of a line block. Based on this information, a worst case two-way processing time delay of 146 bit times was assumed. Bit times are estimated using a trunk data transmission rate of 1200 bps. Delay also had to be assumed for roundtrip HF propagation and delays through the modems, HF and microwave transmitters and receivers and the crypto devices.

At the 1200-bit trunk data rate, a total bit delay was estimated at 100 bits for the round trip path. Thus, we find that out of the 656-bit allowable delay, the nature of the particular data system and propagation path has used up 246 of the bits. This leaves only 410 bits of delay time to be utilized by the error correction devices. For full-duplex operation both paths have to be protected with error correction equipment. This means that the oneway path delay due to error correction coding should not exceed 205 bit times. In practice, a coding device would have to be designed to use somewhat less than the 205 bit times to ensure AUTODIN system compatibility.

The error correction capability of a code is proportional to the amount of processing time a coding device has available and the number of redundant bits the device is allowed to add to the information bit stream. Briefly, an error correction code can correct errors caused by channel disturbances of finite duration by use of redundant bits. The AUTODIN time delay constraint implies that these inter bit dependencies have to be constructed over groups of less than 205 adjacent information bits. To correct errors, the disturbance that causes these errors must be of a duration that is less than the number of bits over which the dependencies have been introduced (in this case, less than 205 information bit times.) How much less is a function of the number of redundant bits that have been added to the information bit stream.

The modem used in this forward error correction program was the AN/USC-10 (V) [4] model 2 previously purchased for use on HF radio circuits. The modem is a 16-tone quartenary differential phase shift keyed modem capable of transmitting serial data at rates of 1200 and 2400 bits per second. As mentioned earlier, a trunk data rate of 1200 bps was used. The modem was operated in the 2400 bps mode. This allowed the addition of one redundant bit for every information bit in the data stream by the coding device.

The problem of testing commercially available coding devices became somewhat

difficult. Under this condition a commercially packaged device had to be available that could meet the AUTODIN time constraints. In addition, DCA was not interested in evaluating coding devices by brand name. Rather, they desired that individual coding techniques be identified and then that a representative of each technique be tested. The desired test outputs were recommendations for data transmission over a future AUTODIN HF overflow and restoral system. These recommendations were to include a specification for a forward error correction device for use on an AUTODIN HF overflow and restoral system.

ANALYSIS OF AVAILABLE FORWARD ERROR CORRECTION EQUIPMENTS

Several electronics companies are in the business of manufacturing equipment to control errors on digital communications channels. Some of these equipments use error detection/retransmission techniques to perform the error correction. Equipments that in any way depend on a retransmission of the message to correct errors were ruled out for the purposes of this test program. The second consideration concerns what is meant by commercially available equipments. We considered only companies that had completely designed and implemented coders and decoders built to good commercial standards that were capable of self-contained operation in the field as of 1 March 1966. In addition, the equipment had to be capable of being maintained by site personnel without the constant supervision of the equipment manufacturer's representatives.

Forward error correction coding devices that met the above criteria were identified as using one of two basic coding techniques to perform error correction, convolutional coding and interlaced or time spread block coding techniques.

The interlaced block coding technique assembles the data stream into t blocks of n bits (see Figure 1). Each block is coded by an (n,k) block code containing k information bits plus r check bits. Transmission is then done serially by columns. In the transmitted stream, bits from alternate code words are interlaced such that bits that were adjacent in the coded word are separated in the transmitted stream by at least t bits. The decoder reassembles the matrix structure of the coded bits and performs the decoding operation. The companies making equipments utilizing this technique use different block codes and variations of the decoding schemes.

The interlaced coding technique, as it applies to this program, has one major drawback. That is the time delay involved in performing the coding and decoding operations. None of the interlaced coding techniques could meet the AUTODIN time delay specifications. For these codes the time delay is a function of the number of bits that must be accumulated in the n x t coding matrix. Available equipment used block codes with n in the range of 14 - 24 bits. The degree of interlace, or the t dimension, is around 200 words or a total storage requirement of greater than 1000 information bits. Obviously, the time required to receive 1000 information bits will exceed the AUTODIN maximum allowable delay time.

Modification of the coding equipment became the only feasible alternative. This requirement to modify the coding equipment conflicted with our criteria for commercially available equipment. The modification required a decrease in size of the n x t coding matrix. Since the (n,k) block code is fixed, this meant cutting down the number of blocks to be interlaced (the t dimension of the matrix).

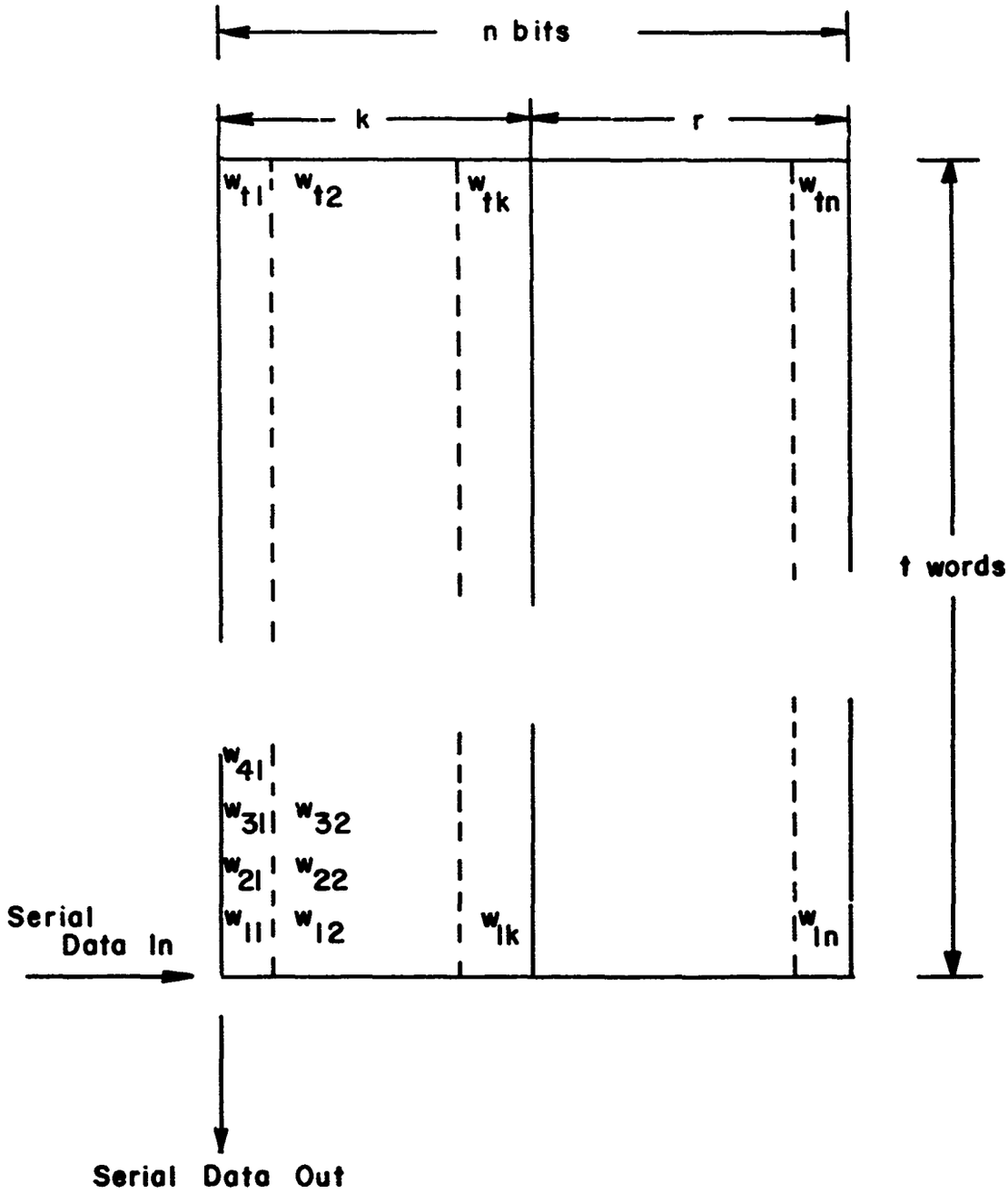

Figure 1. Block Code Interleave Structure

Convolutional coding techniques also introduce a time delay. A rate 1/2 code (one redundant bit for every information bit) introduces a delay of 3n + 4 bits[5] in exchange for the capability of correcting errors caused by a disturbance over a duration of n information bit times.

Our original criteria were relaxed slightly to allow for modification of existing coding equipment to meet an Autodin interface.

A recommendation was made to evaluate three separate coding techniques for possible AUTODIN applications. Based on this recommendation equipments representing a convolutional code, an interleaved (24, 12) block code and an interleaved (24, 12) block code with statistical burst correction were procured for test purposes.

Test Description

A three-phase test program was proposed. The first phase was concerned with determining the error rate of the modem on a transcontinental HF path and the improvement possible by use of the error correction equipments. The second phase involved moving the equipment into AUTODIN terminals and operating in a complete full-duplex AUTODIN environment, utilizing HF radio paths for trunk circuits. The third phase utilized the RADC Digital Communications System Evaluator (DICOSE) facility. The DICOSE[6] facility has the ability to simulate an AUTODIN AESC. In addition, it has the capability of making controlled changes in the AUTODIN operating parameters. This phase was performed to obtain data that would allow recommendations for future AUTODIN terminals.

Phase 1 Error Pattern Test McClellan AFB to Griffiss AFB -

An HF path was established between McClellan AFB in Sacramento, California and Griffiss AFB in Rome, New York (See Figure 2). The Army transmitter facilities at Davis, California were used to transmit the data. (The Davis facility used an AN/FRT-22 with 30kw peak power. Average power was 15-19kw using the AN/USC-10(V) modem). The signal was received at Stockbridge, New York, using two Wullenweber antennas separated by 2500 feet of North-South alignment in space diversity. Stockbridge utilized two Collins 50E-1 receivers.

The transmitted bandwidth was limited to one 3KC sideband. The modem can transmit serial data at 1200 and 2400 bits per second. It can also transmit two independent 1200 bit data streams in DUAL operation. The 16 baseband tones are divided into two 8-tone bands designated as the lower band and the upper band, respectively. 1200 bps data can be transmitted on either the lower band or on the upper band. At 1200 bps the modem can transmit the same data on the upper and the lower bands. In this mode the modem will combine the two received bands, in frequency diversity, to provide one 1200 bps data stream. Transmission at 2400 bps requires all 16 tones. The modem will also accept the output of two HF receivers in space diversity and

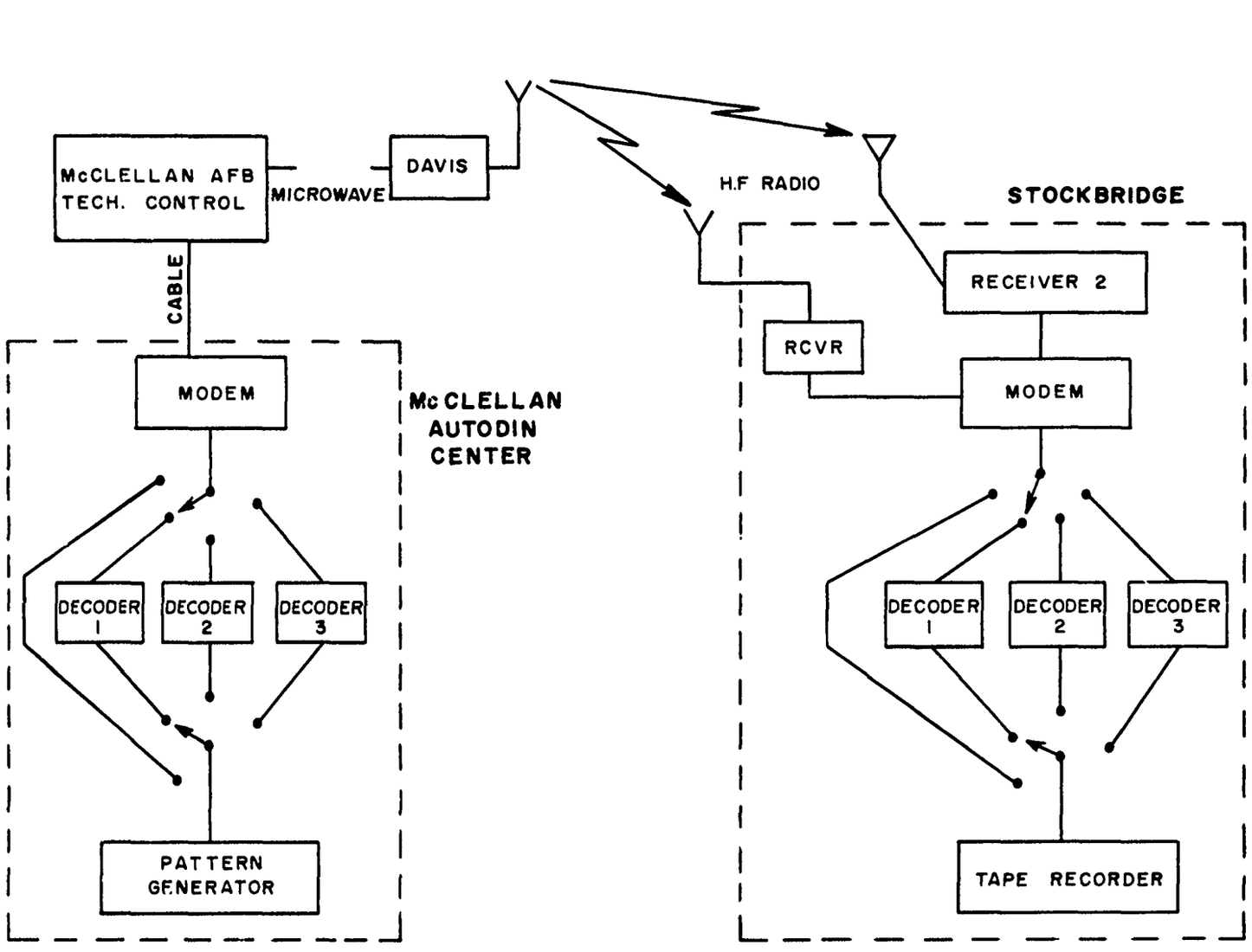

Figure 2. Phase I Test Setup

combine these signals. At 1200 bps two orders of diversity, space and in-band frequency diversity (IBD) are available. At 2400 bps only space diversity is available.

Each of the coding devices used a rate 1/2 code, that is for each data bit introduced a redundant bit was added. A 1200-bps synchronous data stream entering any of the coding devices would emerge as a 2400-bps synchronous data stream.

A linear shift register generated sequence[7] was used as a data source for the Phase 1 tests. A 1200-cycle square wave was presented to this data generator as a timing source. A repetitive pattern is therefore generated as a synchronous bit stream. The length of the shift register, and therefore the length of the repetitive pattern, could be varied by means of a rotary switch. Patterns of length 7, 15, 63, 127, 511 and 1023 were used in this test phase. Data from the pattern generator was either introduced directly into the modem for transmission in the IBD mode at 1200 bps or was introduced into one of the coding devices at 1200 bps. Output from any of the coding devices was entered into the modem for transmission at 2400 bps. The voice bandwidth output of the modem was transmitted via cable and microwave circuits (a distance of approximately 25 miles) to the Davis transmitter site.

The modem and the error correction decoding equipment were located at the Stockbridge receiver site (See Figure 2). The modem output was either an uncoded data stream at 1200 bps with an associated 1200 cycle square wave timing waveform or an error encoded data stream at 2400 bps with its associated 2400 cycle square wave timing. The uncoded data stream and its associated timing were recorded on two tracks of an instrumentation tape recorder using Pulse Duration Modulation (PDM) record amplifiers. The encoded 2400 bps data streams and their associated timing were passed into the appropriate decoding device. The corrected output of the coding devices was a synchronous bit stream at 1200 bps and a 1200 cycle square wave timing waveform. Both the data and the timing outputs of the coding devices were recorded in the same manner as the uncoded data.

Data Analysis

A linear feedback shift register was used to regenerate the exact bit stream that was transmitted. The timing waveform used to drive this shift register was the square wave recorded with the data, either the output of modem or the decoding device. The recorded data stream was compared on a bit-by-bit basis with the regenerated sequence. The recorded data and timing had considerable jitter in it due to phase instabilities in the transmission media, the receive timing correction circuits in the modem and also components of flutter and error in the magnetic tape transports. Although the data contains this jitter, the recorded timing contains the same jitter. When the recorded timing is used to clock the data regenerating shift register the transmitted data and the regenerated data jitter in phase with each other. The transmitted and regenerated data are then compared in a modulo 2 adder. The output of the modulo 2 adder is sampled with the recorded timing signal. The output of this circuit will be a logic "0" when both data bits are the same and a logic "1" when they differ.

The output then is a series of 0's and 1's, with their associated timing waveform, where the 1's represent errors in the received data.

An N stage linear feedback shift register configured to generate a maximum length sequence will provide a sequence of length 2^N-1 before the pattern repeats. This property is used to synchronize the recorded data with the regenerated data. The shift register used to regenerate the sequence has the same configuration (feedback taps) as the transmitter shift register. The first N bits of the recorded data stream are read into the data regenerative shift register. The $N+1^{st}$ bit will then compare favorably with the bit feedback from the regenerative shift register if there are no errors in the first N+1 bits. If there is an error in these first N+1 bits the output of our modulo 2 adder circuit will show a high incidence of logic 1's. A circuit was built to recognize this condition[8]. If the ratio of the logic "1" to logic "0" in 24 adjacent bits exceeded 1/3 the outputs of the modulo 2 adder circuitry are inhibited and the next N recorded bits are entered into regenerating shift register. The process is repeated until synchronization of the two data streams is established. Synchronization can be lost if the modem loses a data bit or a timing bit. This condition is also recognized by the above sync restore circuit and synchronization is re-established.

The error pattern output from the modulo 2 circuitry is further analyzed according to a method suggested by Benice and Frey[9]. The error pattern is blocked off in consecutive, non-overlapping blocks of length M, where M is a power of 2. The error pattern was simultaneously blocked into all M blocks from 2^0 to 2^{11} (Refer to Figure 3). A logic "1" or error, in the error pattern will set all the flip-flops in the top row. The bottom row of flip-flops form a binary counter. A logic "1" appearing in the binary counter will readout and reset its associated flip-flop in the top row. If the output of this flip-flop is a binary "1" it will advance a digital counter associated with that M block length. For a given test run, these counters will total the exact number of M blocks that contain one or more errors.

Computer programs were written from the equations and flow diagrams presented in the Benice and Frey report to obtain the probability that a block of bits of length M is in error for all M between 1 and 2048.

Test Results

Our HF site operation began at 0600 EST and continued until 2400 EST. Once an operating frequency was established we tried to stay with it most of the day. No attempt was made to follow the maximum usable frequency (MUF). Frequency changes were made only after a complete loss of signal or intolerable interference conditions. Over 90 percent of the data was taken at a carrier frequency of 10.995 MHz. Data was taken in the period 9 February 1967 through 12 April 1967.

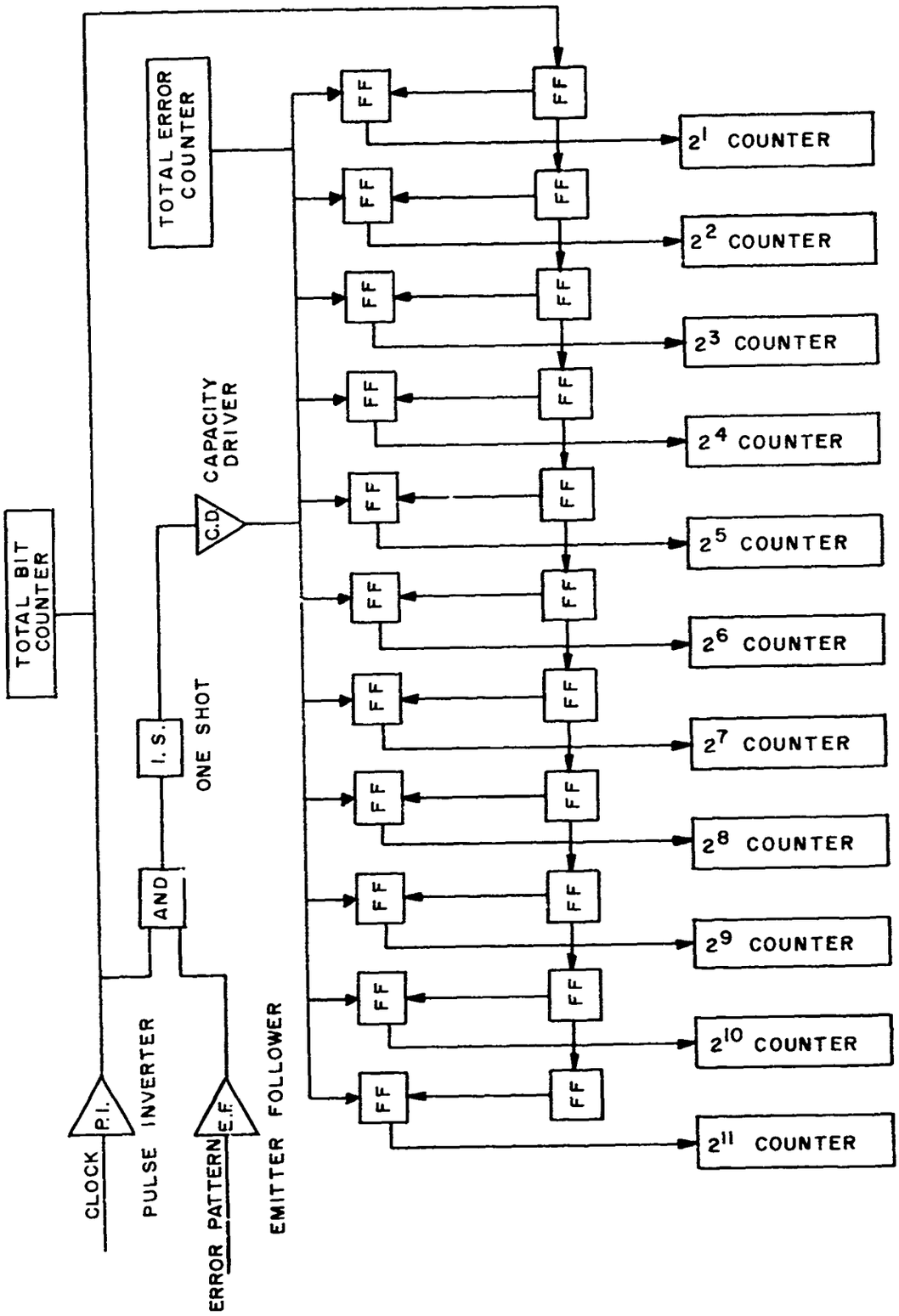

Figure 3. Error Pattern Formatter

A breakdown on the amount of data taken is as follows:

	TOTAL BITS	TOTAL ERRORS
*Uncoded AN/USC-10(V) 1200 bps IBD mode	232,734,750	682,788
*Coder 1 AN/USC-10(V) 2400 bps 2400 mode	131,834,545	125,033
*Coder 2 AN/USC-10(V) 2400 bps 2400 mode	178,101,442	76,611
*Coder 3 AN/USC-10(V) 2400 bps DUAL mode	175,389,037	235,642

Figures 4 thru 7 show the distribution of test runs as a function of the hour of the day. These test sums account for approximately 170 hours of data. We feel the data sample is sufficiently large to calculate the desired statistics.

A word is appropriate at this point concerning what was considered acceptable data. Test runs taken during the time that equipment was malfunctioning were, of course, discarded. If the received data was so garbled that the local pattern generator could not remain in sync, the data was discarded. If the pattern generator could hold sync a high percentage of the time (roughly no more than 7 or 8 momentary sync losses per minute) then the data was considered acceptable. We added the further constraint that a valid test run should consist of a minimum of 1 million consecutive data bits (about 12 minutes of HF data transmission time). With these constraints, short term error rates as poor as 1 error in 30 bits were recorded and analyzed.

A short discussion and analysis of each of the test modes follows:

Uncoded data AN/USC-10(V), 1200 bps I.B.D. -

A base error rate of 2.93 errors per thousand bits (2.93×10^{-3}) was established based on over 53 hours of recorded data. A more important statistic is the probability that an AUTODIN size block (672 bits) will be in error. Figure 8 shows the probability that a block of length n will be in error P(n) for uncoded data. For n equal to 672 bits this value is .1507, that is, approximately 151 blocks out of 1000 will be received in error.

Coder 1 -

This equipment implemented a 23-bit three-error correcting Golay code. An extra bit was added to each sub-block to make a 24,12 rate 1/2 code. The extra bit in each sub-block forming the interleave matrix was used as a synchronization pattern

*Coder 1 is the interleaved 24,12 code
Coder 2 is the interleaved 24,12 code with statistical burst correction
Coder 3 is the convolutional code

Figure 4. Coder 2 Test Run Distribution

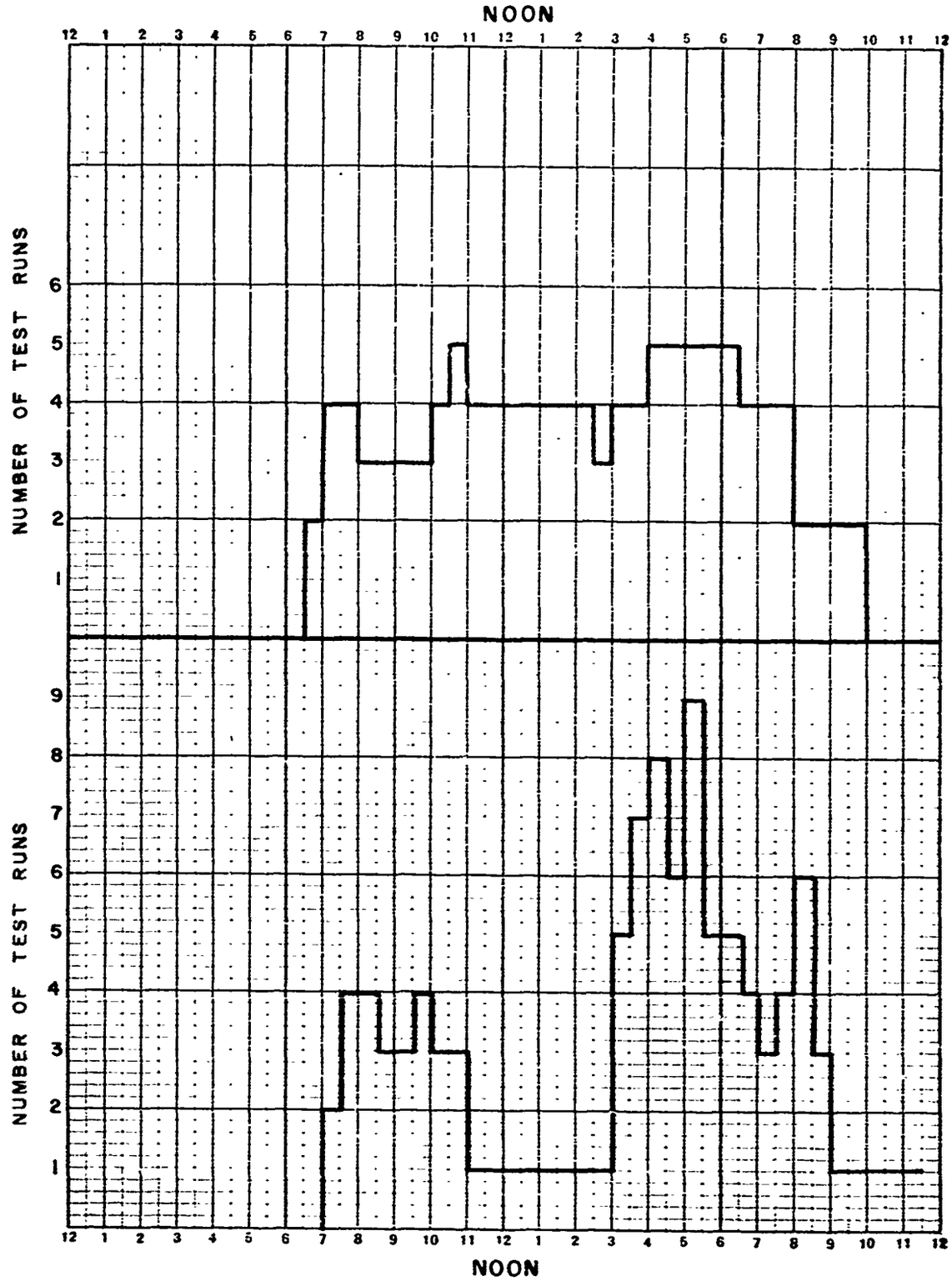

Figure 5. Coder 1 Test Run Distribution

Figure 6. Coder 3 Test Run Distribution

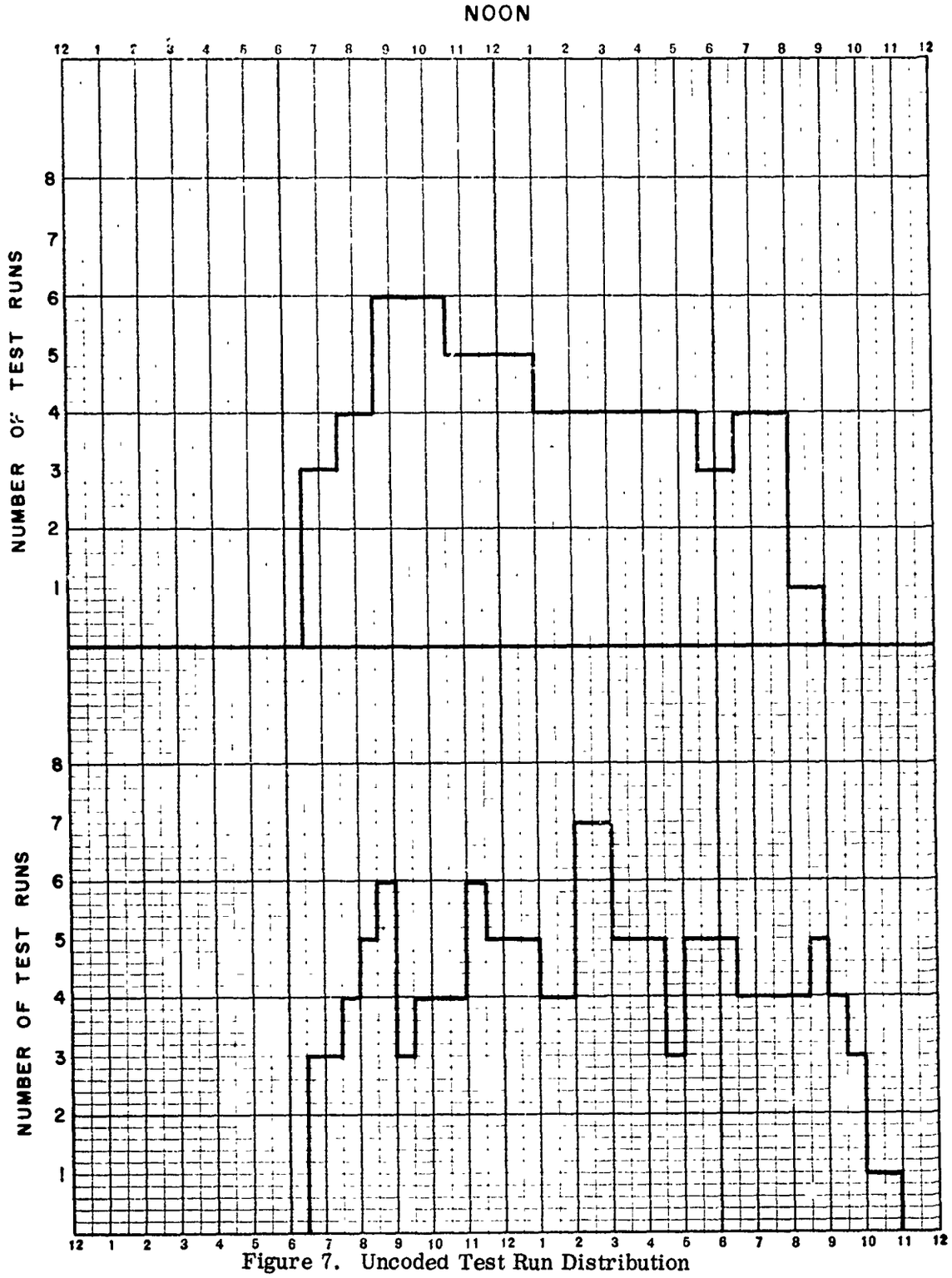

Figure 7. Uncoded Test Run Distribution

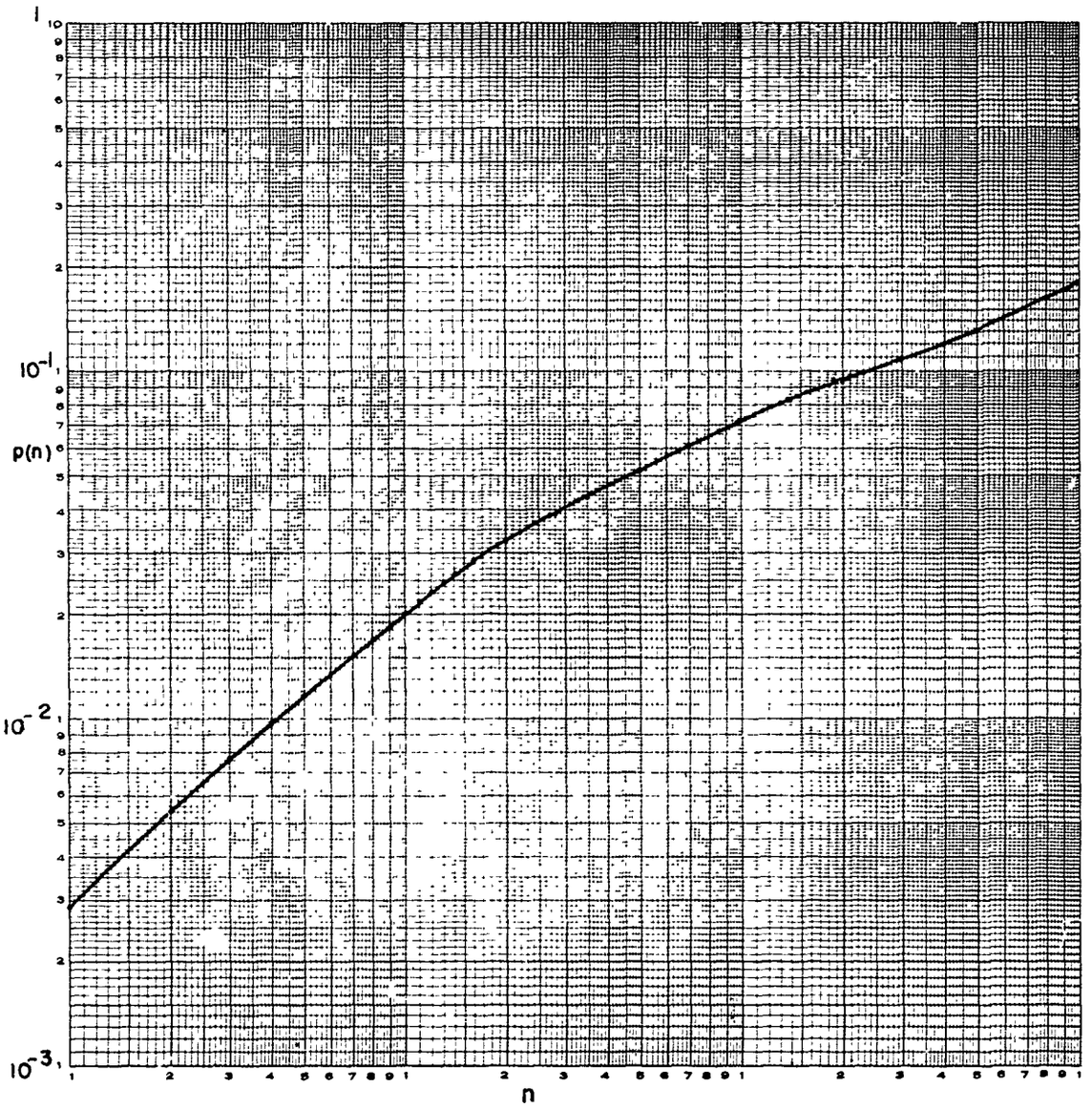

Figure 8. AN/USC-10(V) Modem Uncoded-Predicted Block Error Rate

to obtain block synchronization. The data was transmitted serially at 2400 baud, i.e. between each information bit a redundant bit was transmitted. At the receiver, redundant bits are separated from information bits and error correction is performed. If the modem should lose a bit, then information would be confused with redundancy and the received matrix would have a high error rate. The sync pattern for the next interleave matrix would rectify this situation and the high error rate period would be short lived. The base information error rate utilizing this equipment was 9.48 errors in 10 thousand bits (9.48×10^{-4}). The probability that an AUTODIN size block would be in error is .0623, or approximately 63 blocks out of 1000 received blocks would be in error. Figure 10 displays the probability that an n bit block will be in error P(n) for this equipment.

Coder 2 -

This equipment utilizes a technique similar to the equipment discussed in the section above. It has the additional capability of recognizing a high burst error condition. When this condition exists the decoder does not attempt to decode algebraically. Rather it considers the whole interleave matrix as a large encoded block. It then applies certain statistical properties to correct a burst of errors much longer than normal algebraic decoding could handle[10]. Block synchronization is obtained by operating directly on the redundant bits. The extra bit in each sub-block (see discussion of previous equipment) is not used for synchronization. It is used in this equipment to detect an uncorrectable error condition. Data is transmitted serially at a 2400-bit rate; a redundant bit is transmitted between each information bit. At the receiver, the information is separated from the redundancy and error correction takes place. When the modem loses a bit under these conditions synchronization is lost, and the error rate will remain high. Representatives of this company made a modification to their equipment during the test to rectify this condition. The circuit they added recognized a high error rate condition and resynchronized the decoder. The base information error rate utilizing this equipment was 4.33 errors in 10 thousand bits ($4.33 \cdot 10^{-4}$). The probability that an AUTODIN size block would be in error is .0440 or approximately 44 blocks out of 1000 received blocks would be in error. Figure 11 displays the probability that an n bit block will be in error, P(n) for this equipment.

Coder 3 -

This equipment utilized a convolutional code of rate 1/2. The data was transmitted using the lower band, tones 1 through 8, and the redundancy was transmitted on the upper band, tones 9 through 16, with the modem operating in the DUAL mode. Using this mode, redundant bits are never confused with information bits. The base information error rate using this equipment was 1.34 errors per thousand bits (1.34×10^{-3}). The error rate for an AUTODIN size block was .0828; i.e. about 83 blocks out of 1000 transmitted blocks would be received in error. Figure 9 displays the probability that an n bit block will be in error for this equipment. Figure 12 is a cumulative performance curve. It shows the percentage of time the bit error rate for each of the

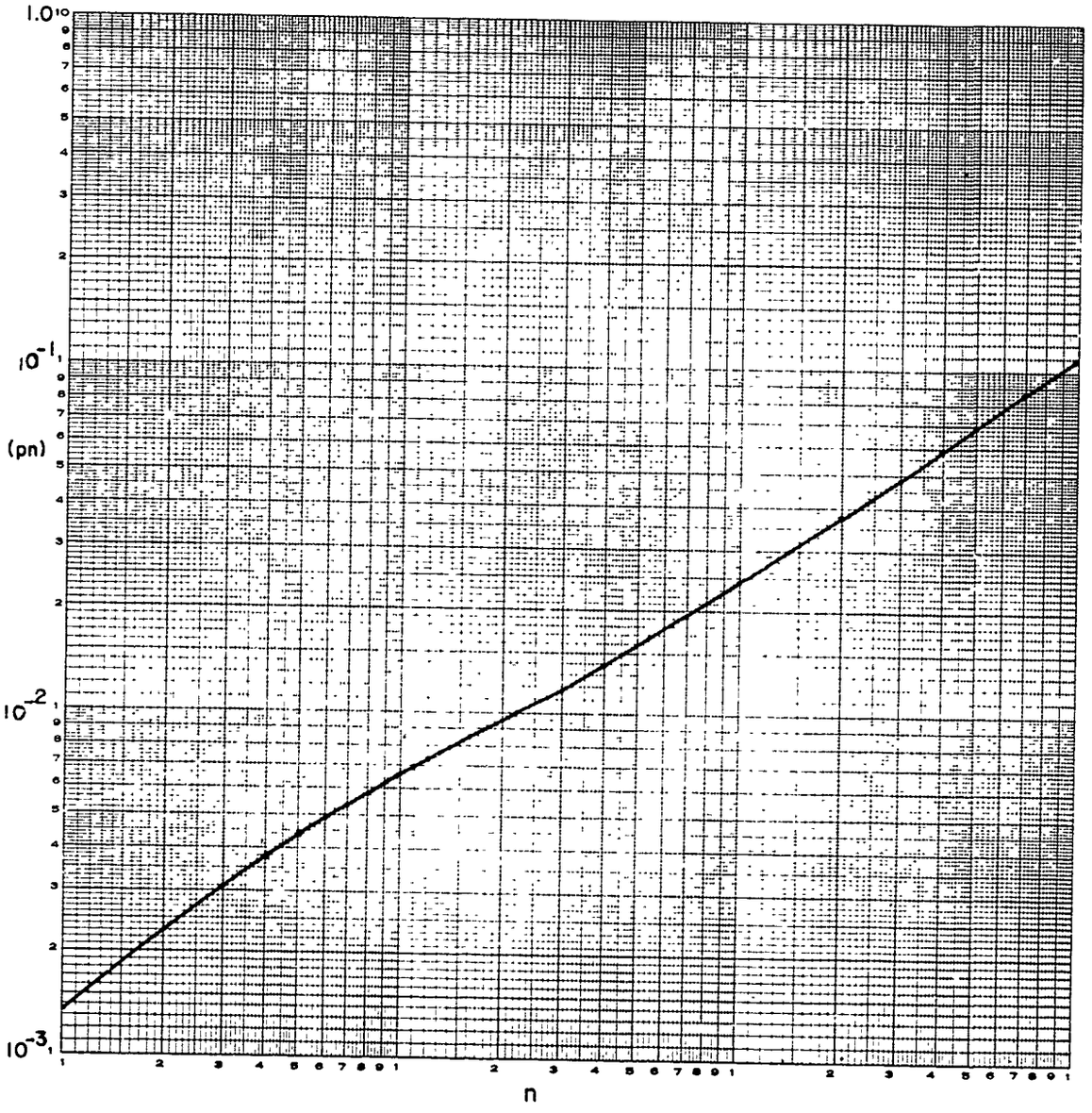

Figure 9. Coder 3 AN/USC-10(V) Modem Predicted Block Error Rate

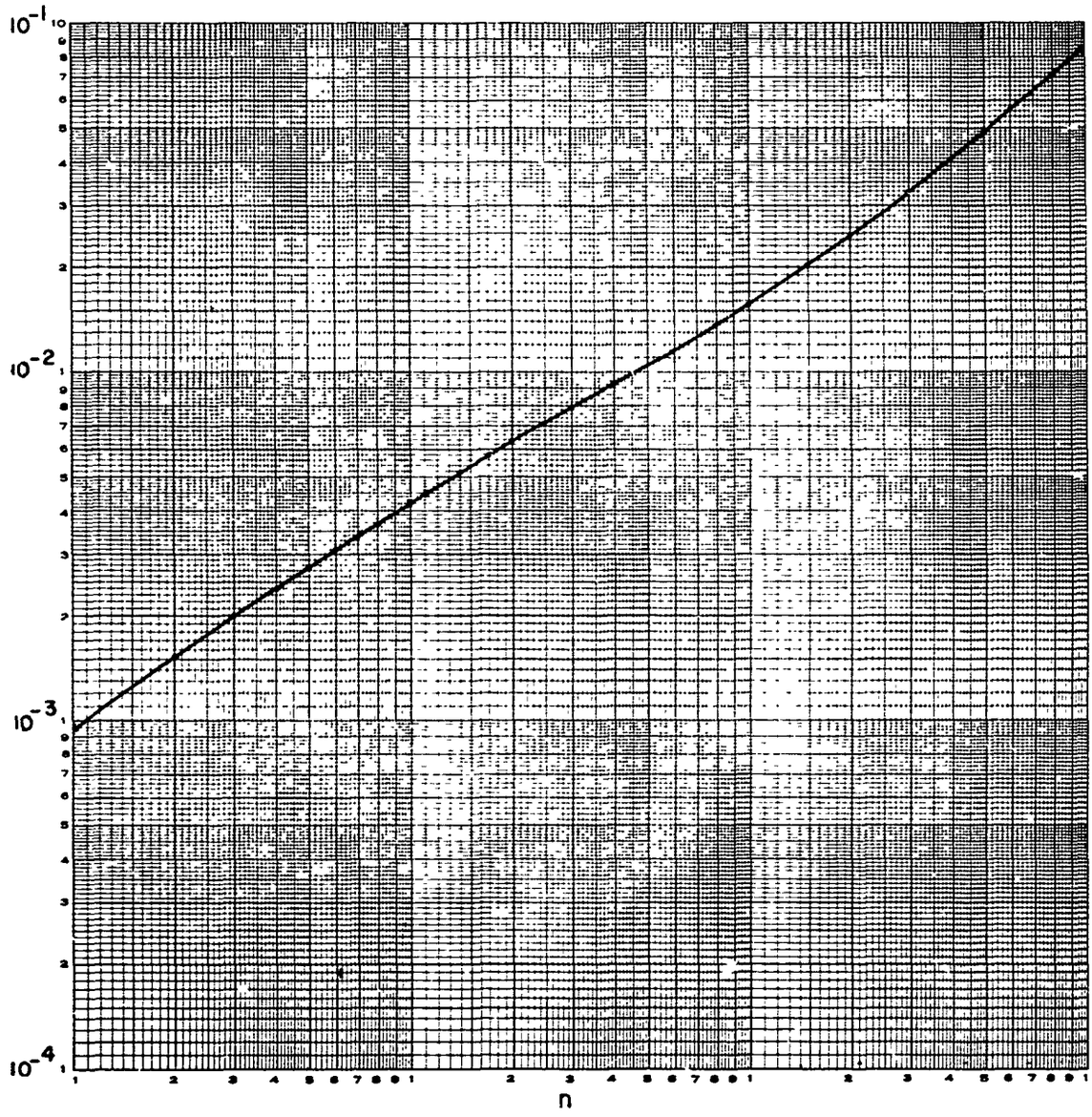

Figure 10. Coder 1 - AN/USC-10(V) Modem - Predicted Block Error Rate

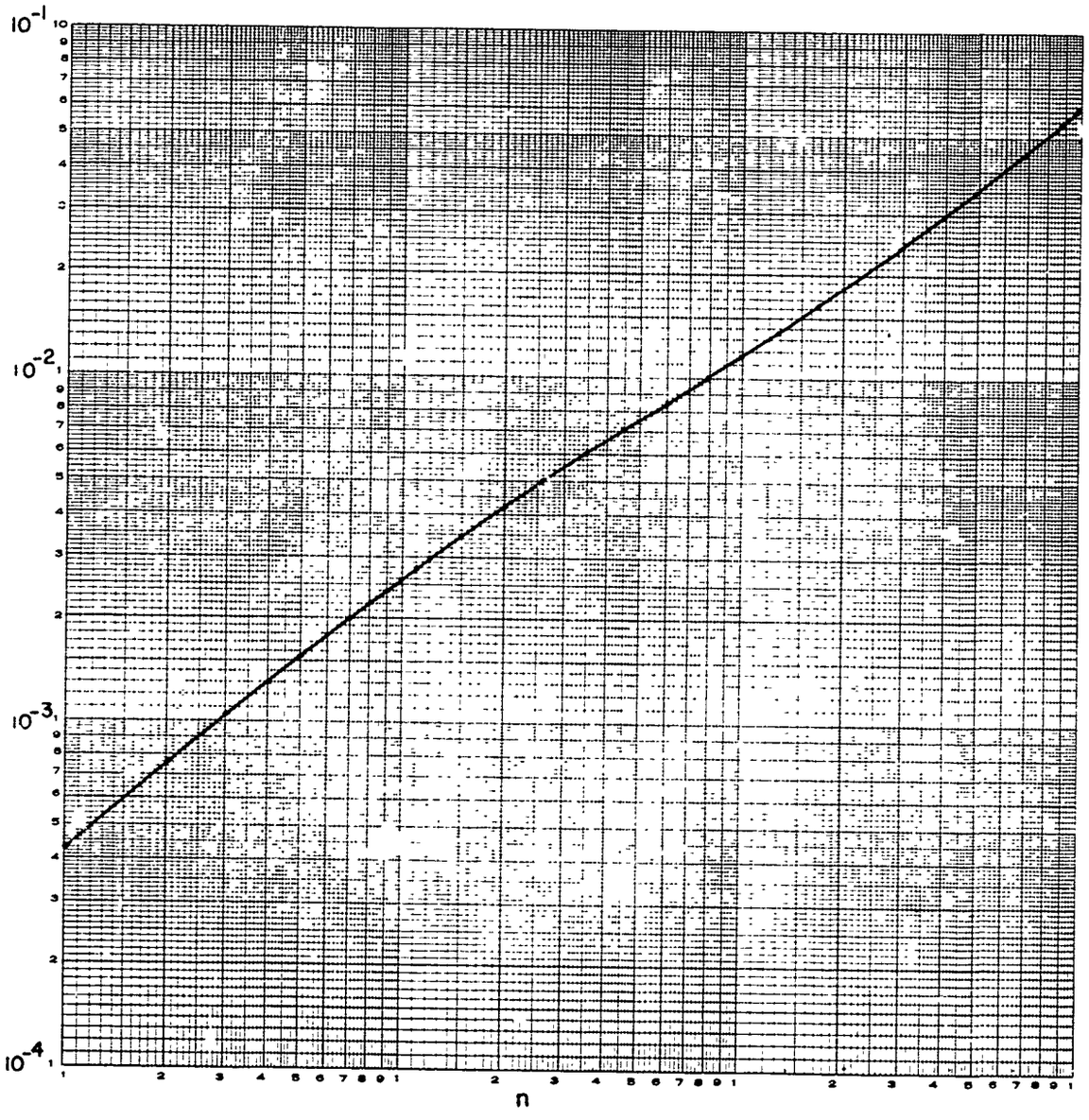

Figure 11. Coder 2 AN/USC-10(V) Modem - Predicted Block Error Rate

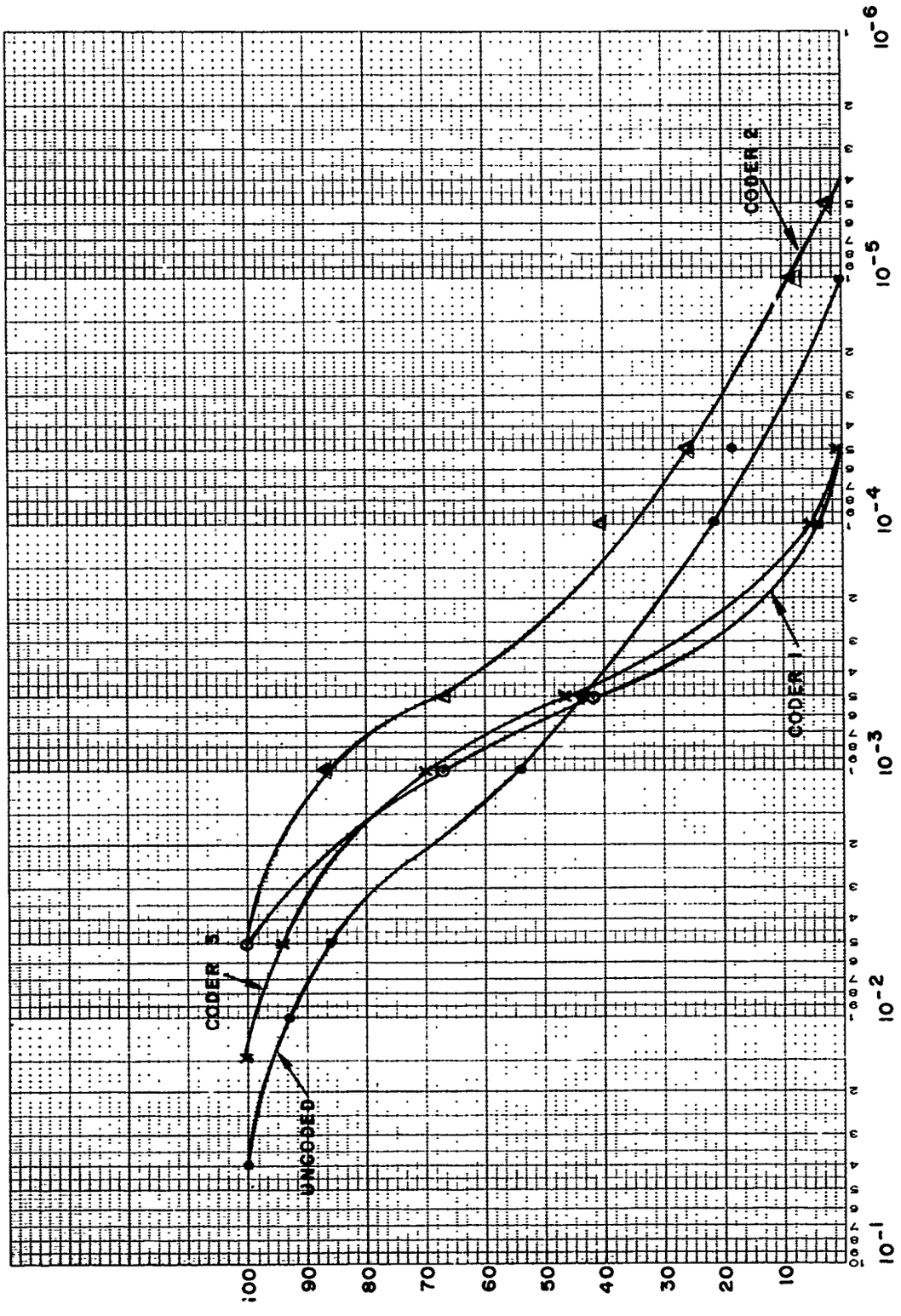

Figure 12. Cumulative Performance Chart

devices tested was less than or equal to the value shown on the abscissa. The curve was obtained by first calculating the average error rate for each test run and then figuring the percentage of the total bits included in that test run. As mentioned earlier, the minimum test run was 12 minutes. The maximum test run was just under 105 minutes. For the uncoded data, no test run contributed more than 3.2% or less than 0.86% of the total uncoded data taken. For coder 1 these figures are 5.3% for the longest run and 0.9% for the shortest. Corresponding figures for coder 2 are 3.94% and 0.68%. For coder 3, the maximum and minimum test run lengths are, respectively, 4.36% and 0.65% of the total information bits processed by this coder.

Phase II - Full Duplex Trunk Operation in an AUTODIN Environment

The AUTODIN AESC terminals at McClellan AFB and at Hancock Field, Syracuse, N. Y. were utilized in this phase of the test program (See Figure 13). Hancock Field is approximately 30 miles from the Griffiss AFB HF receiver site at Stockbridge. Three-schedule 4C telephone lines connected the Stockbridge site with the Hancock Field terminal. Two of these lines were used to carry the dual space diversity signals directly to the modem at Hancock. The third telephone line carried transmitted data to the Stockbridge site. From Stockbridge, the transmitted traffic went to the Griffiss AFB HF transmitter site at Ava, N. Y. via a microwave path. Ava is approximately 25 miles north of Stockbridge. The HF radio path was between Ava and the US Navy receiver site at Skaggs Island, California. Skaggs Island was connected to McClellan AFB via two microwave channels for diversity operation. The Ava transmitter site used a Collins Radio 205J-1 transmitter with 45 KW peak power. Average power was 18-22KW using the AN/USC-10(V) modem. The transmit antenna was a Log-Periodic steerable oriented at 270°. The Skaggs Island receiver site utilized two double ended rhombic antennas oriented at 74° to feed an AN/FRR 60V in dual diversity. The transmission path from McClellan AFB to Stockbridge was the same path as was used in the Phase I tests.

For full-duplex operation, two data encoders (transmitters) were kept on the West Coast and one encoder was shipped to the East Coast. The corresponding decoder was shipped to McClellan. The two interleave coding devices were tested in the west-to-east leg and the convolutional coding equipment was tested in the east-to-west path. Most of the test consisted of alternating between the two interleaved coding devices on the west-to-east path and alternating between convolutionally encoded data and uncoded data in the east-to-west path. Some uncoded data, however, was taken in the west-to-east path.

Two 50-block messages were entered into the AUTODIN system at the McClellan AESC. A unique message routing indicator was assigned for use in this test. The McClellan switch recognized this routing indicator as a Hancock address. The test messages underwent normal AUTODIN processing up to and including the crypto device (KG-13). The serial bit stream emerging from the KG-13 was entered either into the forward error correction device undergoing test or directly into the modem if an uncoded data test were being performed. The data at this point was a synchronous

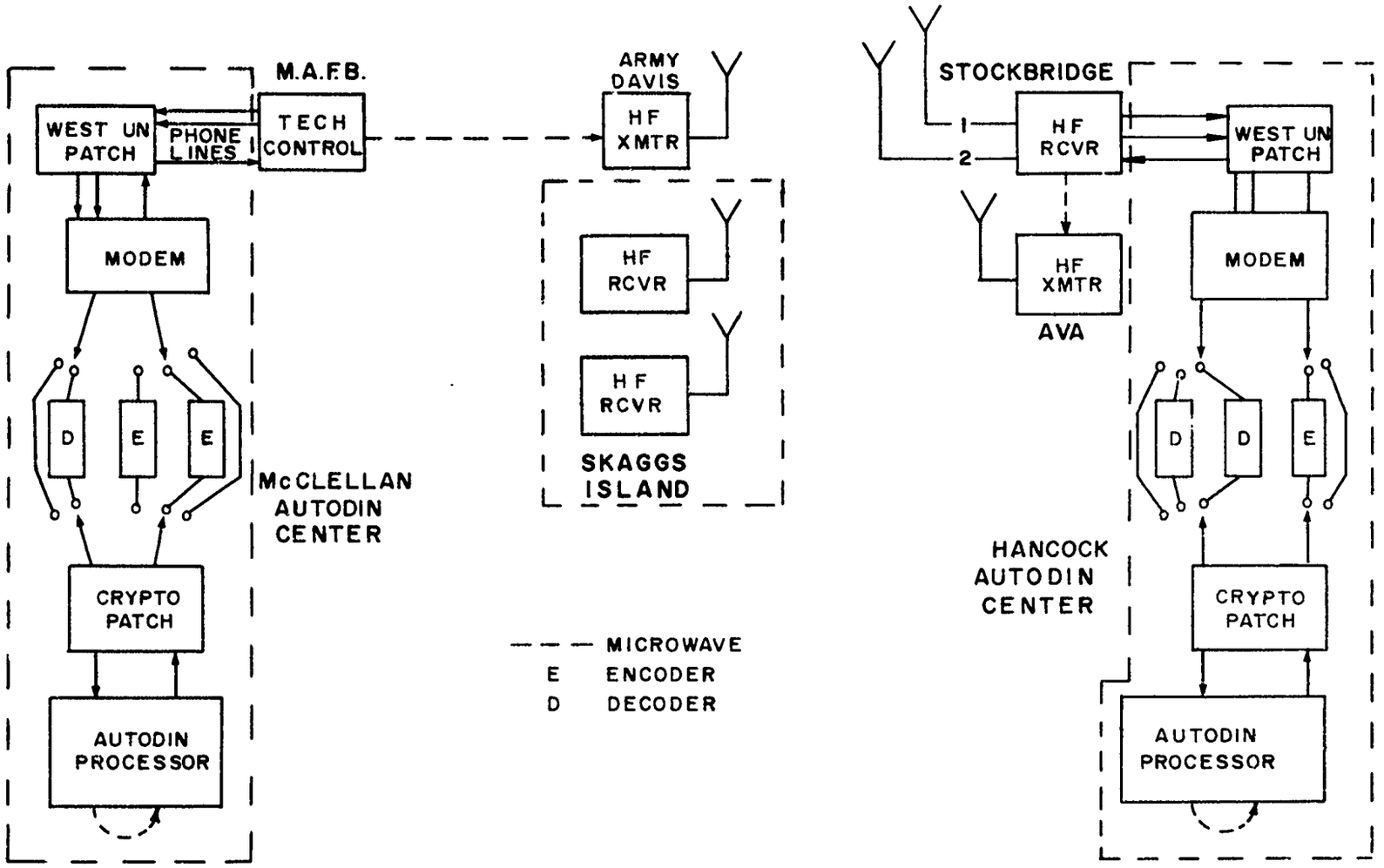

Figure 13. Phase II Test Set-up

serial stream at 1200 bps. The AESC provided in-phase square wave timing signals at 1200 and 2400 Hz. Uncoded data was transmitted at 1200 bps in the IBD mode to gain an order of diversity. In this operation, only the 1200 Hz timing was provided to the modem. For coded operation, timing at 2400 Hz was provided to the encoding device and to the modem. The bit stream emerging from the encoding device was a synchronous bit stream at 2400 bps. This data was entered into the modem and transmitted in the 2400 bps mode.

At the Hancock terminal, data from the modem is either at 2400 bps or at 1200 bps with its associated timing waveform. Encoded data is passed through the appropriate error correction equipment. The bit stream from the error correction devices is at 1200 bps. Data at 1200 bps and associated timing was presented directly to the crypto device at Hancock. Normal AUTODIN message processing occurred from this point on. The Hancock AESC was programmed to recognize the unique routing indicator as a McClellan address. The Hancock switch then re-routed the message through a similar path back to the data modem. Data at this point is always at 1200 bps. The convolutional coding device did not utilize a timing signal. It accepted the data asynchronously and strobed it internally. As in Phase I, this device provided two data streams at 1200 bps. This information was transmitted in the DUAL mode. Timing from the Hancock AESC at 1200 Hz was always provided to the modem. As before, uncoded data was transmitted in the IBD mode.

The two messages were continuously passed between the two AUTODIN switches. All message blocks were acknowledged over the return path. Block retransmission, as required, followed normal AUTODIN operating procedures.

Test Procedure -

Each morning, a full duplex HF radio circuit was established by the technical controllers at McClellan AFB and the Griffiss AFB receiver site at Stockbridge. Once the circuit was established, it was turned over to the Western Union AUTODIN technicians at McClellan and Hancock. These technicians patched in the error correction devices being tested, established crypto set and started message traffic moving over the circuit. The circuit remained under the control of these technicians and the AUTODIN tech controller until the circuit degraded to the point where the AUTODIN technicians felt that a frequency change was needed. In this case, the technical controllers at McClellan and Stockbridge were notified and the above process was repeated. Usually the inability to maintain crypto set dictated a need for a change in frequency.

Data Analysis -

The Hancock terminal ran the off-line statistics (OLS) daily for our channel. This raw data provided the number of 50 block messages transmitted and the number of blocks in error at both the output and the input of the Hancock switch. This information was provided on an hourly basis.

Off-Line Statistics (OLS) were not available from the McClellan switch. At periodic intervals during the day the AUTODIN technician was able to obtain a cumulative block error count for the channel input and output. These data were correlated with the station logs at the Hancock terminal, the McClellan terminal and the HF receiver site at Stockbridge.

The data analyzed was for those periods when all of the station-logs indicated a fully operational channel was available. This data is summarized in the following tables.

TABLE 1 - ANALYSIS OF DATA BY DATE

Week of May 1 thru May 5

Hancock AESC			McClellan AESC	
Good Blocks Received	Error Blocks Received	Date	Good Blocks Received	Error Blocks Received
0	0	May 1	0	0
5350	77	May 2	5350	48
1800	117	May 3	2050	27
3000	139	May 4	3000	22
5150	142	May 5	5200	4
15,300	475		15,600	101

Hours of Operation

May 1	0	hours
May 2	6	hours
May 3	2 1/2	hours
May 4	6	hours
May 5	5 1/2	hours
	20	hours

WEEK OF MAY 8 THRU MAY 12

Hancock AESC			McClellan AESC	
Good Blocks Received	Error Blocks Received	Date	Good Blocks Received	Error Blocks Received
2100	172	May 8	2150	14
4450	271	May 9	4500	109
10,500	911	May 10	10,600	10
10,100	2174	May 11	10,100	2
5600	4041	May 12	5700	310
32,750	7569		33,050	445

Hours of Operation

May 8	2	hours
May 9	5 1/2	hours
May 10	9 1/2	hours
May 11	9 1/2	hours
May 12	9 1/2	hours
	36	hours

WEEK OF MAY 15 THRU MAY 19

Hancock AESC			McClellan AESC	
Good Blocks Received	Error Blocks Received	Date	Good Blocks Received	Error Blocks Received
13,450	1678	May 15	13,550	9
4,050	906	May 16	4,200	21
9.050	948	May 17	9,050	71
1,150	117	May 18	1,200	6
5,200	113	May 19	5,500	133
32,900	3,762		33,500	240

Hours of Operation

May 15	9	hours
May 16	5 1/2	hours
May 17	7	hours
May 18	3	hours
May 19	6	hours
	30 1/2	hours

WEEK OF MAY 22 THRU MAY 26

Hancock AESC			McClellan AESC	
Good Blocks Received	Error Blocks Received	Date	Good Blocks Received	Error Blocks Received
0	0	May 22	0	0
0	0	May 23	0	0
1850	927	May 24	1900	177
6100	263	May 25	6300	188
0	0	May 26	0	0
7950	1190		8200	365

Hours of Operation

May 22	0
May 23	0
May 24	4 hours
May 25	5 hours
May 26	0
	9 hours

TABLE 2 - ANALYSIS OF DATA BY CODING DEVICES

West to East Path

Coder 2			Coder 1		
Date	Good Blocks Received	Error Blocks Received	Date	Good Blocks Received	Error Blocks Received
May 2	5350	77	May 9	4450	271
May 3	1800	117	May 10	10,500	911
May 4	3000	139	May 11	10,100	2174
May 5	5150	142	May 24	1850	927
May 8	2100	172	May 25	6100	263
May 15	13,450	1678		33,000	4546
May 16	4050	906			
May 17	9050	948			
May 18	1150	117			
May 19	5200	113			
	50,300	4409			

Uncoded Data		
May 12	5600	4041

Hours of Operation

Coder 2	52 1/2 hours
Coder 1	33 1/2 hours
Uncoded	9 1/2 hours

EAST TO WEST PATH

Coder 3			Uncoded		
Date	Good Blocks Received	Error Blocks Received	Date	Good Blocks Received	Error Blocks Received
May 2	5350	48	May 9	4500	109
May 3	2050	27	May 10	10,600	10
May 4	3000	22	May 11	10,100	2
May 5	5200	4	May 12	5700	310
May 8	2150	14	May 24	1900	177
May 15	13,550	9	May 25	6300	188
May 16	4200	21		39,100	796
May 17	9050	71			
May 18	1200	6			
May 19	5500	133			
	51,250	355			

Hours of Operation

Coder 52 1/2 hours

Uncoded 43 hours

The hours of operation are somewhat deceiving. They included periods when crypto synchronization was lost. Crypto re-set is done manually and requires telephone coordination between the two terminals. This procedure will eat into the time recorded under hours of operation. Many times a crypto set is not obtained at the first try. If crypto set could not be obtained after 15 to 30 minutes of trying, then the HF Tech Controllers were asked to obtain a better channel. This was done only as a last resort. A frequency change required, on the average, an hour to an hour-and-a-half to perform, with no guarantee that the new frequency would be any better. Our policy, therefore, was to try to operate through a poor transmission condition until the condition proved to be not of a temporary nature.

From examination of Table 2, it is obvious that the East-West and West-East paths were not equivalent and could not be considered as reciprocal paths. Comparison of the coding devices used on separate paths becomes impossible. We can, however, measure the degree of improvement of a coding device versus uncoded data on the same channel. In the case of the two interleaved coding devices, a valid comparison can be performed. Unfortunately, poor propagation conditions during the last week of testing prevented our obtaining more data on the uncoded West-East path.

A block error rate calculation can be performed by dividing the number of error blocks received by the total number of blocks received. The AUTODIN system requires the retransmission of the two data blocks whenever a data block is received in error. The total number of blocks received would then be the number of good blocks received plus two times the number of error blocks received:

$$\text{Block Error Rate (BER)} = \frac{\text{Cumulative Block Error Count (CBEC)}}{\text{Good Blocks Received} + 2\ (\text{CBEC})}$$

Calculations for the West - East path

Coder 2

$$\text{BER} = \frac{\text{CBEC}}{\text{Good Blocks} + 2\ (\text{CBEC})}$$

$$= \frac{4409}{50,300 + 2\ (4409)} = .07458$$

Coder 1

$$\text{BER} = \frac{4546}{33,000 + 2\ (4546)} = .108$$

Uncoded Data

$$BER = \frac{4041}{5600 + 2\,(4041)} = .29535$$

Calculations for the East - West path

Coder 3

$$BER = \frac{355}{51,250 + 2\,(355)} = .00683$$

Uncoded Data

$$BER = \frac{796}{39,100 + 2\,(796)} = .01956$$

Table 3 Phase II block error rate compared with the Phase I predicted error rate for an AUTODIN size block.

Phase II Block Error Rate		Phase I Predicted Block Error Rate
Coder 2	.07458	.044
Coder 1	.108	.0623
Uncoded	.29535	.1507

Another possible calculation would be an improvement factor calculated as a function of the uncoded block error rate. We have defined this factor as the block error rate for uncoded data divided by the block error rate for coded data on the same channel. These improvement factors are as follows:

$$\text{Improvement Factor} = \frac{\text{Uncoded block error rate}}{\text{Coded block error rate}}$$

$$\text{Coder 2} = \frac{.29535}{.07458} = 3.96$$

$$\text{Coder 1} = \frac{.29535}{.108} = 2.66$$

$$\text{Coder 3} = \frac{.01956}{.00683} = 2.86$$

This improvement factor is compared with the improvement factor predicted by the Phase I data in the following table.

TABLE 4

Phase II Improvement Factor		Phase I Predicted Improvement Factor
Coder 2	3.96	3.42
Coder 1	2.66	2.42
Coder 3	2.86	1.82

In each case the improvement factor was larger than that predicted by the Phase I data. In the case of Coder 3, we found that the improvement was significantly larger. The Coder 3 device was tested over the better side of the full duplex channel. This result would tend to confirm the results of the MITRE/ESD Eastern Test Range HF coding tests which indicate that the coding improvement factor increases as the base error rate improves to 1×10^{-3} or 1×10^{-4}. This result is also implied in a Codex report to the NASA AMES Research Center titled "Phase I Report On A Study of Coding For Deep Space Telemetry", October 1965.

In the period of 1 May through 26 May, the AUTODIN data switches were made available for a total of 200 hours. In an attempt to identify problem areas in interfacing the AUTODIN system into an operating HF radio circuit, the channel usage information from the station logs was abstracted and is presented in the following charts.

	Operating	Frequency Changes	Error Correction Equipment	High Frequency Equipment	Environ-mental Equipment	Personnel Errors	Natural Disturbances
1 May				Antenna Check at Ava		Misunderstanding as to which terminal should orig. msg.	
Time	1540-1900	1210-1220 0700-0800		1140-1510		1540-1845 0805-1130	
Hours Out		1 hr 10 min		3 hr 30 min		7 hr 30 min	
2 May						Cannot contact Skaggs Island	
Time	1030-1330 1615-2000	1000-1030 1210-1220				1330-1600	
Hours Out		40 min				2 hr 30 min	
3 May							Kind Unknown
Time	0940-1010 1030-1100 1143-1330 1540-2000	1123-1130 1330-1430					0715-0930
Hours Out		1 hr 10 min					2 hr 15 min
4 May					Air Cond. Down at Hancock Fld		
Time	0855-1230 1410-1600 1620-2000	1230-1255 0700-0840 1600-1620			1240-1400		
Hours Out		2 hr 25 min			1 hr 20 min		

	Operating	Frequency Changes	Error Correction Equipment	High Frequency Equipment	Environ-mental Equipment	Personnel Errors	Natural Disturbances
5 May			Coder not operating	Recvr change at Skaggs Island			
Time	1020-1305 1615-2000	0700-0930	0800-1000 1310-1410	1450-1610			
Hours Out		1 hr 30 min	3 hr	1 hr 20 min			
8 May				Repair Ant. Matrix Ava	Telco Line 171 (Stock-bridge to Hancock) Microwave M. AFB		
Time	1510-1825	0700-0930 1050-1100 1130-1140 1320-1430		0940-1045	1300-1400		
Hours Out		3 hrs		1 hr 5 min	?		
9 May							
Time	1040-1510 1639-1900	0700-1000 1510-1630					
Hours Out		4 hr 20 min					

	Operating	Frequency Changes	Error Correction Equipment	High Frequency Equipment	Environ-mental Equipment	Personnel Errors	Natural Disturbances
10 May							
Time	1015-1430 1517-1900	0700-0900 1430-1510					
Hours Out		2 hr 40 min					
11 May				Repair Receiver M. AFB			
Time	1030-1900	0700-0835		0835-1000			
Hours Out		1 hr 35 min		1 hr 25 min			
12 May							
Time	0947-1400 1422-1900	0700-0940 1400-1420					
Hours Out		3 hr					
15 May							
Time	0925-1100 1110-1837	0705-0915 1100-1110					
Hours Out		1 hr 20 min					
16 May				Ant. Check Ava			
Time	0825-1330 1635-1900	0700-0825 1330-1530		1530-1630			
Hours Out		3 hr 25 min		1 hr			

	Operating	Frequency Changes	Error Correction Equipment	High Frequency Equipment	Environ-mental Equipment	Personnel Errors	Natural Disturbances
17 May			Coder not keying				
Time	0933-1100 1238-1900	0700-0930	1110-1238				
Hours Out		1 hr 30 min	1 hr 30 min				
18 May					ADUs down M. AFB		
Time	0850-1215	0700-0850 1600-1900			1230-1600		
Hours Out		4 hr 50 min			3 hr 30 min		
19 May							
Time	0829-1130 1310-1900	0700-0815 1130-1310					
Hours Out		3 hrs					
22 May							Unknown
Time		0830-1540					0830-1700
Hours Out		7 hr 10 min					
23 May							SID
Time		0830-1700					0830-1700
Hours Out		8 hr 30 min					8 hr 15 min

	Operating	Frequency Changes	Error Correction Equipment	High Frequency Equipment	Environmental Equipment	Personnel Errors	Natural Disturbances
24 May					ADU Problem (Han)		
Time	1154-1550	0830-0900 1550-1625			1135-1215		
Hours Out		1 hr			45 min		
25 May							
Time	1135-1700	0830-1135					
Hours Out		3 hrs					
26 May							Auroral Residue
Time		0830-1700					0830-1700
Hours Out		8 hr 30 min					8 hr 30 min
Total Hrs of Phase II							
186 hr 55 min	94 hr 30 min	35 hr 15 min	4 hr 30 min	8 hr 20 min	5 hr 35 min	10 hr	27 hr 45 min

The charts account for approximately 187 out of the total of 200 hours. The remaining time was lost in setting up the equipment each morning and stowing it each evening during the 20 days of operation. The four-and-one-half hour time change to defective error correction equipment is somewhat deceptive. In each case the coders failed because of improper timing signals provided to them. The personnel running the test were AUTODIN technicians and engineers charged with the daily operation of the AUTODIN Switches. We sacrificed some operating time by following this policy due to inadequately trained personnel. We did gain some valuable insight concerning system integration by letting the AUTODIN technicians interface directly with the operators of the HF radio channel.

Our largest time loss was charged to changing radio frequencies. We operated with only one transmitter and two receivers in diversity operation for each side of the full duplex circuit. In normal operation, a hot standby transmitter should be made available to reduce the time needed for a frequency change. Further time could be cut from changing frequencies if there were one system technical controller to maintain the entire circuit. During this test the AUTODIN technical controllers had to interface with the HF radio technical controllers in order to request a change in channel operating parameters. The individual technical controllers had no appreciation for the problems of his counterpart at either the AUTODIN switch or the radio center. We would recommend that the AUTODIN technical controllers be trained in the rudiments of HF radio technical control and then allowed direct contact with transmitter and receiver sites.

The second largest channel downtime charge was due to natural disturbances. We suffered a Sudden Ionospheric Disturbance (SID) on the 23rd of May that completely wiped out reception on all frequencies on the west coast. An aurora on the 26th of May made it impossible to receive anything at the Stockbridge receiver site. The other natural disturbances were due to poor propagation and interference from other radio sources that could not be avoided by changing frequency. This is something that must be lived with and taken into consideration when reliability of an HF radio backup for AUTODIN is discussed.

Ten hours were charged to personnel errors. This time would have been reduced to a negligible amount if the AUTODIN operators had been adequately trained in the operation of the coding devices and the modems.

Downtime due to HF radio equipment was all in terms of routine maintenance. In a normal operational condition, this could be avoided by proper scheduling of maintenance.

AUTODIN Interface

The CONUS AUTODIN system was designed to operate on carefully equalized telephone line and microwave circuits. Data at 2400 bits per second is transmitted asynchronously through the system. The data stream at the receive terminal is

re-timed at the receive terminal by recognizing the bit transitions. This technique works well on data transmitted over the phone line network but is completely inappropriate for use on HF radio. There can be ± 70μsec jitter on each 32-bit frame within the data modem. This time difference was possibly the cause of the sync adapter circuits losing bit synchronization. This problem was resolved by bypassing the sync adapter circuits and providing the data and timing signals from the modem directly to the crypto device. Although the timing and data signals contain considerable jitter, the negative going edge of the timing signal is always maintained in the center of the data bit. This criterion is sufficient to maintain the crypto in sync. We would recommend that this procedure be followed whenever AUTODIN traffic is transmitted over HF radio.

Synchronization of the cryptos in the AUTODIN system is done manually and requires the coordination of the operator at both the send and the receive terminals. A loss of crypto synchronization can also go unnoticed for a period of time. Since loss of crypto sync occurs much more frequently on HF radio circuits, the obvious recommendation would be to install automatic re-sync circuitry, possibly triggered by a time-out signal, on all HF circuits used for AUTODIN traffic. If this is not feasible, a second recommendation would be to install audio and visual alarm circuits triggered by a loss of crypto set. Something will be needed along these lines to improve the channel efficiency figure.

Conclusions

The Phase II tests have demonstrated the value of error correction coding in an AUTODIN HF back-up system in terms of AUTODIN block error rate and channel utilization efficiency. Although improvement factors in the range of 2.66 to 3.96 appear small, this improvement is for a block of 672 data bits. A close look at Table 2 will show how important this improvement factor is in terms of the number of line blocks transmitted per unit time. The uncoded data experienced almost as many error blocks in one day of operation as one of the coding equipments experienced in its entire operational period. This improvement is further demonstrated by comparing the data taken on May 11 with the data taken on May 12. On May 11, we operated with an interleaved coder in the West-East path. We had 9-1/2 hours of channel operation and lost 3 hours because of frequency changes and a bad receiver. In this time we passed 10,100 good blocks and 2,174 bad blocks for a total, including retransmissions, of 14,448 line blocks. On May 12, we operated uncoded in the same path. We again had 9-1/2 hours of channel operation and 3 hours of down time due entirely to frequency changes. This day we passed 5,600 correct blocks and 4,041 errored blocks. The total, including retransmission, was 13,682 line blocks transmitted. From all indications, propagation conditions were about equal, with May 11 and May 12 being two of the better days for transmission.

The difference in performance for the two days can be attributed directly to the coding device. The difference in the total number of line blocks transmitted in the two days was 766 blocks. We feel that this figure represents the ability of the coding equipment to maintain traffic during periods of poor propagation. The gain with coding is therefore two-fold. A gain is experienced in the overall block error rate and the total amount of time that a channel can be utilized is increased through the use of a coding device.

Phase III - DICOSE Simulation of AUTODIN Operation -

For this third phase of the test program the DICOSE facility was used to simulate both the transmit and receive AUTODIN terminals. All of the coding equipments, encoders and decoders, were transferred to the DICOSE center at Griffiss AFB, Rome, N. Y. The center was connected to the Stockbridge receiver site by three cable and microwave circuits; one circuit for transmission and two for diversity reception as in Phase I and Phase II operations. The HF radio paths from Ava to Skaggs Island and from Army Davis to Stockbridge were connected in tandem. Data received at Skaggs Island was regenerated through the AN/USC-10(V) modem at McClellan AFB before transmission from the Davis transmitter site. (See Figure 14 for Phase III test set-up).

The DICOSE processor was programmed to simulate an AUTODIN transmit and an AUTODIN receive terminal. The two terminals operated independently of each other. Message traffic, originated at the transmit terminal, was transmitted over the radio path and was received at the receive terminal. The message was acknowledged over a hardwire connecting the simulated transmit and receive terminals. A crypto device (KG-13) was used only in the path containing the two HF radio links.

The messages transmitted were of the structure described in the earlier section on AUTODIN Time Constraint. Line blocks were transmitted continuously and the AUTODIN time constraint was imposed on all line blocks. The REP character sequence was not used. If the answer timer expired before an ACK or NACK sequence was received, a time-out counter was incremented and the message was reinitiated. One hundred consecutive time-outs would stop the program and advise the operator to check the channel.

The receive terminal was programmed to search for the Start of Header (SOH) or Start of Text (STX) character. Upon recognizing either of these characters, the receive terminal would begin to read the remainder of the 84-character block. Each character was checked for parity, with even parity for control characters and odd parity for data characters. A character parity error would flag the NACK sequence and increment a character parity error counter. Separate counters totaled control character parity errors and data character parity errors. As soon as the 84th character (the block parity character) was checked, the ACK 1, ACK 2 or NACK sequence as appropriate, was initiated.

In addition to totalizing the number of time-outs, the simulated transmit terminal also counted the number of ACK 1, ACK 2 and NACK sequences received and the total number of blocks transmitted.

The simulated receive terminal also counted the number of good blocks received and the number of longitudinal parity errors.

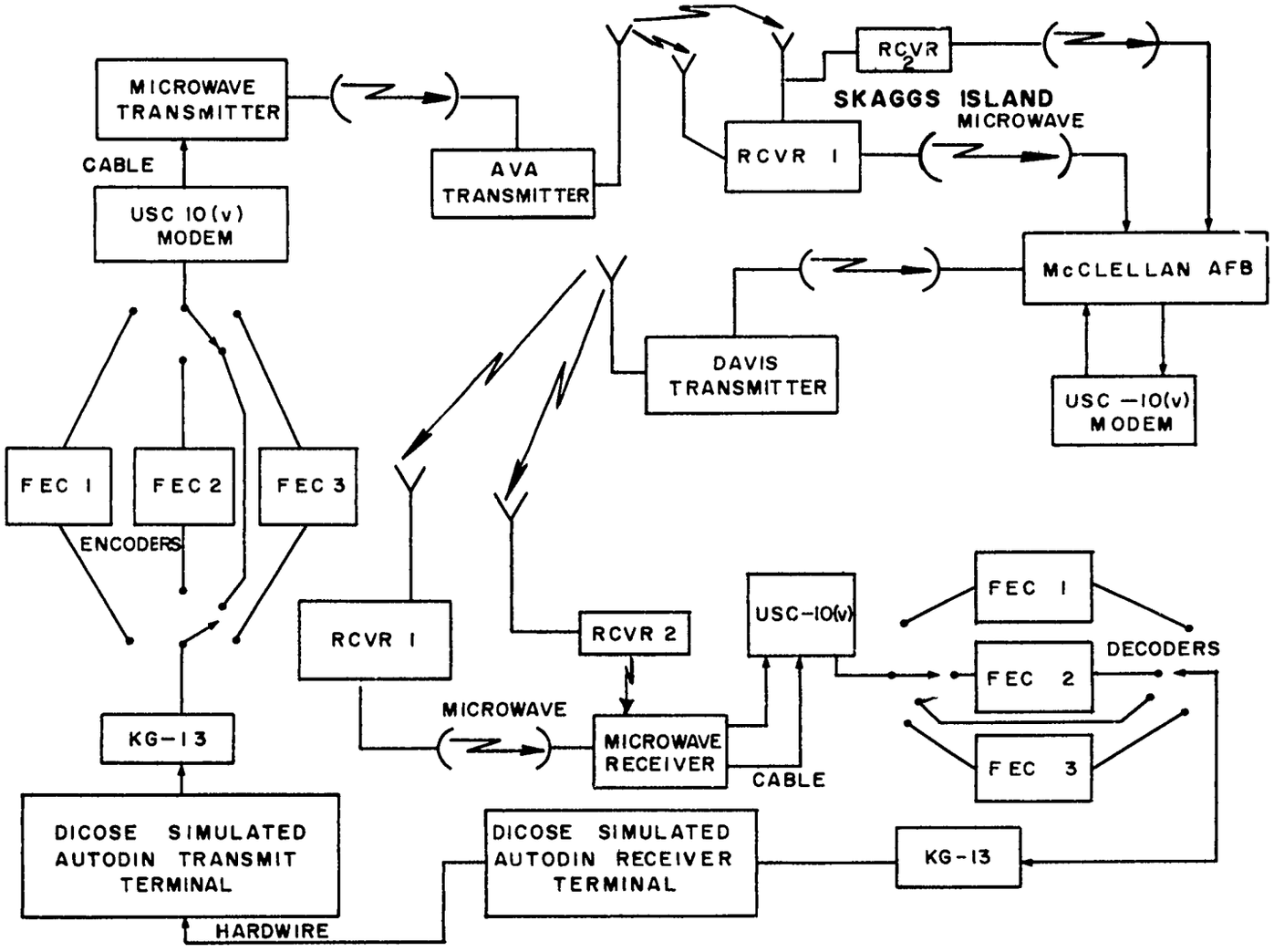

Figure 14. Phase III Test Set-up

Another output feature of the program was the bit propagation delay time or the time that the DICOSE processor transmitted the first bit of a control character until that bit was again received by the DICOSE processor. This time was presented to the nearest millisecond. These time calculations were made for all coding devices with and without the HF circuit and also for the DICOSE processor backed up on itself. This data is presented in the following tables.

TABLE 5 - PROPAGATION TIMES WITHOUT RADIO PATH

DICOSE - DICOSE (2400 bps)	4 ms
DICOSE - DICOSE (1200 bps)	8 ms
DICOSE - Modem - Modem - DICOSE (2400 bps)	31 ms
DICOSE - Encoder 1* - Decoder 1* - DICOSE	266 ms
DICOSE - Encoder 2** - Decoder 2** - DICOSE	230 ms
DICOSE - Encoder 3*** - Decoder 3*** - DICOSE	24 ms

* Coder 1 is the interleaved (24, 12) code
** Coder 2 is the interleaved (24, 12) code with Statistical Burst Correction
*** Coder 3 is the convolutional code

Since all of the coding devices accept data and present it to the data sink at the 1200 bit per second rate, the calculation for the processing delay time for each of the coding devices and the modem is straightforward.

Coder 1	258 ms
Coder 2	222 ms
Coder 3	16 ms
Modem (2400 bps)	27 ms

TABLE 6 - PROPAGATION TIMES WITH RADIO PATH (INCLUDING MODEM REGENERATION IN CALIFORNIA)

DICOSE - Modem - Modem - DICOSE (2400 bps)	100 ms
DICOSE - Encoder 1 - Modem - Modem - Decoder 1 - DICOSE	362 ms
DICOSE - Encoder 2 - Modem - Modem - Decoder 2 - DICOSE	325 ms
DICOSE - Encoder 3 - Modem - Modem - Decoder 3 - DICOSE	124 ms
DICOSE - Modem - Modem - DICOSE (1200 bps)	107 ms

From Table 5 and Table 6, the radio propagation delay time for the tandem HF path (including the microwave links) can be calculated. The first two results in Table 6 indicate a radio path propagation delay time of 42 milliseconds. The third result provides a delay time of 41 milliseconds which is within the 1 millisecond error tolerance in our measuring equipment. The fourth and fifth results in Table 6 provide a slightly different delay time. In these cases the modem was operating at 1200 bps. The same 16-tone baseband package was transmitted through the radio path as in the case of the 2400 bps data. We can safely assume that the propagation delay for the analog signal is 42 milliseconds in both cases. We then come to the conclusion that the modem takes slightly longer to process data at 1200 bps than at 2400 bps. Performing the arithmetic, we find that the delay through two modems at 1200 bps is 58 ms or a delay of 29 ms through each modem. Using the values derived from Tables 5 and 6, we can calculate the total path delay for a full duplex circuit implemented in both paths by each of the coding devices.

Coder 1 -

Delay through 2 modems at 2400 bps	54 ms
Delay through 2 encoders plus 2 decoders	516 ms
Round trip propagation delay	42 ms
	612 ms

Coder 2 -

Delay through 2 modems at 2400 bps	54 ms
Delay through 2 encoders plus 2 decoders	444 ms
Round trip propagation delay	42 ms
	540 ms

Coder 3 -

Delay through 2 modems at 1200 bps	58 ms
Delay through 2 encoders plus 2 decoders	32 ms
Round trip propagation delay	42 ms
	132 ms

These figures are important when they are compared with the AUTODIN time delay constraints discussed in an earlier section. In full duplex operation, an ACK or NACK character must be received by the transmit terminal prior to the transmission of the 83rd character of the second line block. When operating in the full duplex mode the transmit terminal must also simultaneously ACK and NACK the distant terminal with which it is communicating. In practice, then, when two terminals are transmitting line blocks to each other in the continuous mode, each transmit terminal must transmit an ACK or NACK sequence for each line block received. In the continuous mode, one line block will be received each time a line block is transmitted. This will cause the transmit terminal to multiplex a two-character ACK or NACK sequence into the transmitted bit stream. Since the transmission speed remains constant (1200 bps) this requirement will add the transmission time of two characters to the AUTODIN time delay constraint, i.e. the transmit terminal must receive an ACK or NACK from the distant terminal within the time that it takes to transmit 82 characters of the next line block plus a two character ACK or NACK sequence or a total delay constraint of 84 characters. An 84-character delay at 1200 bps is 560 milliseconds.

It is obvious that this time delay would have been exceeded if both sides of the full duplex circuit had been protected by Coder 1.

If both sides of the full duplex circuit were protected by Coder 2, the time delay constraint would have been violated whenever the AUTODIN processing delays exceeded 20 milliseconds.

Coder 3 with a total delay of only 132 milliseconds should never exceed the AUTODIN time delay constraints.

Results From AUTODIN Simulation -

The data from the DICOSE simulated transmit and receive terminals are presented in the following table. The DICOSE simulator separated the character errors into control character errors (the LMF or security character and the end of line blocks or end of message character) of which there are two per line block, vertical parity errors (data character errors) and longitudinal parity errors (errors in the parity check character caused by errors in the data characters).

TABLE 7

	RECEIVE TERMINAL					TRANSMIT TERMINAL				
	Control Errors	Vertical Parity Errors	Longitudinal Parity Errors	Error Blocks	Correct Blocks	Transmitted Blocks	ACK 1 Received	ACK 2 Received	NACK Received	Timeouts
Coder 1	6065	129,130	10,322	10,365	135,384	148,748	67,697	67,686	10,355	2995
Coder 2	5172	106,872	5,534	5,547	129,998	132,597	64,997	64,984	5,531	2474
Coder 3	5997	142,782	13,401	13,425	106,035	124,692	53,027	53,000	13,417	5219
Uncoded Data	8227	183,831	27,465	27,545	93,324	126,347	46,651	46,638	27,493	5448

The answer timer was set at 546 milliseconds, the transmission time for 82 eight bit characters at a transmission rate of 1200 bps. The longest path delay was 362 milliseconds, measured when Coder 1 was used in the path. Theoretically, the answer timer should never have expired. If an error occurs in the Start of Header or Start of Text character (the block frame character) the receive terminal will not read the line block. The receive terminal will wait until a valid SOH or STX character is received before it will read in the corresponding line block. When this occurs a line block will be lost, the answer timer will expire, the message will be reinitiated and the time-out counter incremented. One hundred consecutive time-outs were always caused by a loss of HF circuit or a loss of crypto sync. When this happened, the program would stop and the accumulated data would be printed out. Each time this happened, one hundred counts would be subtracted from the number of time outs and the number of blocks transmitted before the data was recorded.

Data print-outs were taken approximately once each hour. Each time a print-out was taken, the transmit and receive terminals would be momentarily closed to incoming data. This would cause the loss of a line block at the receive terminal and the loss of an ACK or NACK sequence at the transmit terminal. This explains why the number of transmitted blocks does not equal the sum of the number of received blocks plus the number of time outs. A similar discrepancy can be seen in the number of error blocks and NACK sequences and the number of correct blocks and the sum of ACK 1, ACK 2 sequences. Each time the data was reinitiated: at the start of day, after each print-out or after a timeout the receive terminal would respond with an ACK 1 sequence for the first correct line block received. This explains why the number of ACK 1 sequences is always slightly larger than the number of ACK 2 sequences.

Data Analysis

From Table 7 the following error rate calculations are presented.

$$\text{Received Block Error Rate} = \frac{\text{Error Blocks Received}}{\text{Total Blocks Received}}$$

Coder 1	.0711
Coder 2	.0409
Coder 3	.1124
Uncoded	.2279

The following table compares the error rates as predicted in Phase I and as experimentally determined in Phases II and III.

	Phase I - Predicted Block Error Rate	Phase II - Block Error Rate	Phase III - Block Error Rate
Coder 1	.0623	.108	.0711
Coder 2	.0440	.07458	.0409
Coder 3	.0823	---	.1124
Uncoded	.1507	.29535	.2279

It is interesting to note that although the Phase III data was taken over a two-link HF path or a radio path of twice the length of the Phase I and Phase II data the error rate for an AUTODIN size data block remained essentially the same. This would tend to indicate the value of end-to-end error correction with data regeneration at the nodes of tandem radio paths.

A block error rate improvement factor can be calculated and compared with the test results from the other phases.

$$\text{Improvement Factor} = \frac{\text{Uncoded Block Error Rate}}{\text{Coded Block Error Rate}}$$

Coder 1	3.21
Coder 2	5.57
Coder 3	2.03

	Phase I - Predicted Improvement Factor	Phase II - Improvement Factor	Phase III - Improvement Factor
Coder 1	2.42	2.66	3.21
Coder 2	3.42	3.96	5.57
Coder 3	1.82	2.86	2.03

The Phase III improvement factor is larger in the cases of Coder 1 and Coder 2 than in either Phase I or Phase II. The Coder 3 data on Phase II is not readily compared with the other data. Coder 3 did show an improvement on Phase III as compared with the Phase I data.

Table 7 provides the total number of good line blocks received. Typical AUTODIN operation would require the retransmission of two line blocks every time one block is received in error. The number of correct new line blocks received would be the number of good blocks received minus the number of error blocks received.

	New Line Blocks Received Correctly
Coder 1	125,019
Coder 2	124,451
Coder 3	92,610
Uncoded	65,779

With this figure an efficiency calculation is possible.

$$\text{Efficiency} = \frac{\text{New Line Blocks Received Correctly}}{\text{Blocks Transmitted}}$$

Coder 1	.8405
Coder 2	.9386
Coder 3	.7427
Uncoded	.5206

An idea of the information transfer rate of each coding device on this circuit can be obtained by dividing the number of good new line blocks received by the hours of operation.

When the channel was in service data was transmitted in the continuous block mode at 1200 bps under the AUTODIN time constraint. Since the circuit delay times for all of the Phase III tests were well within the time delay constraint, block transmission was continuous during periods in which the channel was available. The total transmission time available can then be calculated by dividing the number of blocks transmitted by the hourly block transmission rate. An 84-character AUTODIN block

contains 672 bits. At the 1200 bps rate it requires 560 milliseconds to transmit one block. At this rate 6428 blocks can be transmitted in one hour. The hours of operation are as follows:

Coder 1	23.14 hours
Coder 2	20.63 hours
Coder 3	19.40 hours
Uncoded	19.66 hours

Throughput -

Coder 1	5402 good new line blocks per hour
Coder 2	6032 good new line blocks per hour
Coder 3	4773 good new line blocks per hour
Uncoded	3345 good new line blocks per hour

An interesting calculation that provides some insight into the effectiveness of each coding device is the average number of character errors (vertical parity errors plus control errors) contained in blocks that are in error. (See Table 7). This figure provides an indication as to how badly a line block must be in error before the coding device will fail to correct it.

	Average Character Errors/Block in Error
Coder 1	13.043
Coder 2	20.199
Coder 3	11.022
Uncoded	6.973

The calculation for uncoded data is of course meaningless in the context of coder effectiveness. It does provide a measure of the degree of error clustering on the channel used, and a measure of the improvement possible with each of the coding devices tested. The calculations are not quite accurate. The character errors listed under vertical parity errors in Table 7 are only those characters that contain an odd number of errors. The characters with an even number of errors (2, 4, 6 or 8 errors) will have correct parity and will not be tabulated. The true values for character errors per block in error will be slightly larger than those given above.

Modem Bit Synchronization

Throughout the three phases of the test program, we were plagued by the problem of the modem losing bit synchronization. This problem was more apparent in our Phase II and Phase III operations where a crypto device was used in the circuit. When the modem loses bit sync the crypto will also drop synchronization and must be reset before valid data can be passed. A portion of the Phase III effort was devoted to determining what made the modem lose bit synchronization.

The receive section of the modem derives bit synchronization from the received 16 tone analog signal. The 16 data tones in the baseband package are separated by 110 cycles. At approximately the middle of the baseband spectrum one frequency is left blank; i.e. data tone number 8 is at 1485 Hertz and tone number 9 is at 1705. Spaced 110 cycles from tone 8 and tone 9 at a frequency of 1595 Hertz, no energy is transmitted. The receive portion of the modem searches for an energy null around 1595 Hertz. The modem's capability of tracking an energy null around 1595 Hertz allows it to correct for frequency shift and phase dispersion in the HF path. The resultant tracking signal is used to correct or update the modem's internal oscillator. In the absence of a received signal (a deep fade), the received portion of the modem will be clocked by the internal oscillator.

Two test configurations were set up to experimentally determine what made the modem lose bit synchronization. The first set-up used the DICOSE terminal, the crypto device and the modem. The baseband signal was looped back into the modem and the data returned over the same path to the DICOSE processor. The second test set-up was the same as used in all Phase III data taking and is shown in Figure 14.

We first attempted to force the modem to lose bit synchronization by interrupting the baseband signal between the transmit and receive portions of the modem. The signal was interrupted for periods as long as ten minutes in both of the test configurations. In no case were we able to cause the modem to lose bit sync by interrupting the signal. The crypto output would of course be in error during the time the signal was removed from the modem. As soon as the signal was restored to the modem, the modem would lock back into synchronization and the crypto output would be correct.

We next tried to force the modem to lose synchronization by introducing noise into the modem's analog signal. The maximum output of a noise generator was added into the modem tone package. In the second test configuration (using the radio paths) the noise was added both prior to transmission and after reception. The maximum noise generator output was not used when added into the transmitted signal. Care had to be taken to keep from overdriving the exciter. Again, we were unable to force the modem to lose bit synchronization by the addition of gaussian noise. As in the case of interrupting the signal, the crypto output would be in error for as long as the noise was added to the signal. As soon as the noise was removed the modem would lock into bit synchronization and the crypto output would be correct.

We were able to force the modem to lose bit synchronization by adding a tone at a frequency near 1595 Hertz to the received analog signal. In the first test configuration (modem operating back-to-back), the modem could be forced to lose sync by the addition of a tone in the frequency range of 1540 to 1630 Hertz. As the interfering tone approached 1595 Hertz, less power was required in the interfering tone to drive the modem out of bit synchronization. In the second test configuration (signal transmitted over the radio path) the interfering tone could force the modem out of bit synchronization over a frequency range of 1522-1672 Hertz.

Apparently the major cause of bit synchronization loss throughout the test period was QRM.

Conclusions and Recommendations

This three-phase test program demonstrates the feasibility of using HF radio as an overflow and restoral circuit for AUTODIN operation when used in conjunction with a forward acting error correction code. Data transmission, although possible without error correction, is not recommended. Channel efficiency without coding is only 52 percent as compared with 93 percent with one of the coding devices. The throughput or new good line blocks received per hour average about one-half of what could be expected when the circuit is protected by a coding device. (Phase II and Phase III data).

Our Phase III effort demonstrated the need for fully trained operators and a single technical controller for both the AUTODIN system and the HF radio path. During Phase II, the test was conducted by the AUTODIN operational personnel and the technicians and engineers who normally run the HF circuits. The radio people were unfamiliar with the AUTODIN problems. The AUTODIN technicians were ignorant of the vagaries of HF data transmission, the modem, and the coding devices. Control of the modem, coders, and the data switch was the responsibility of the AUTODIN Tech Controller. HF radio discipline, frequency changes, and preventative maintenance were under the control of the HF radio tech controller.

The complete Phase III operation was under the control of a single test director who had complete authority to handle problems associated either with the data switch or with radio propagation. The technicians and engineers were thoroughly trained in modem and coder operation and, perhaps more important, were motivated toward the success of the test.

Based on our Phase II and Phase III results, we would recommend that the sync adapter circuitry presently used at the CONUS AUTODIN switches be bypassed and both data and timing be provided to the data sink by either the modem or the coding device as applicable.

A major source of channel downtime on all three test phases was a loss of bit synchronization. This was more obvious on Phases II and III where a loss of bit sync will cause a corresponding loss of crypto synchronization. Loss of crypto sync is sensed only by the operator. We would recommend that automatic re-sync circuits for the cryptos be implemented or, if this is not feasible, that audio and visual alarms be provided to indicate that the channel has lost bit synchronization. We would not recommend a change in the modem's method of bit synchronization until a comparative test is performed with other bit synchronization techniques. Concerning the coder modem interface, we would recommend that the modem be operated in the DUAL mode with the encoder providing two 1200 bps bit streams. One of these bit streams should be the unencoded data; the second bit stream should be the calculated redundancy. In this manner, the decoding device would never confuse information bits with redundant bits and would lessen the probability of the decoder losing synchronization.

The purpose of this test program was to evaluate commercially available coding equipment for possible use on an HF AUTODIN overflow and restoral circuit. Representative coding devices for each of the distinguishable coding techniques were procured and a comparative test performed. Based on our test results and the stated purpose of this test effort, we would have to choose the technique represented by Coder 2, the interleaved block code with the statistical burst error correction, as the one which consistently shows the best performance in each of the test phases. Coder 2 out-performed Coder 1 in block error rate performance on all three phases. It exceeded the Coder 1 throughput rate on the phases where this statistic could be measured. This performance was attained even though the Phase III results showed that Coder 1 used a processing delay time that would preclude its use in full-duplex AUTODIN operation. As mentioned earlier, the error correction capabilities of a coding device are proportional to the amount of processing time a coding device is allowed and to the number of redundant bits the coding device may add to the information bit stream. Coder 2 out-performed Coder 1 even though the processing delay through Coder 1 was more than 15 percent greater than the processing delay through Coder 2.

Coder 2 out-performed Coder 3 in all categories of measurement where the two coders were tested on the same circuit. Coder 3 did not utilize the full processing time available. This was unfortunate. It was, however, the only commercially available convolutional coder that would meet the AUTODIN constraints. There is no information to indicate that a more sophisticated convolutional coder would out-perform the interleaved (24, 12) code with statistical burst correction.

We have but one reservation in recommending a coding device designed around the technique represented by Coder 2 for use in AUTODIN HF overflow and restoral operation. Our Phase III data shows that Coder 2 when implemented in full duplex AUTODIN operation would allow only 20 milliseconds for data processing by the end terminals. We feel that this not a large enough safety margin. The coder should be re-designed to increase this factor to the range of 25 to 30 milliseconds.

Reference 3 provides the cumulative processing delay times for two AUTODIN switches in full duplex operation. The average processing time between two line blocks in the same message is 22 milliseconds. The worst-case processing time delay is 132 milliseconds. To force the coding device to leave sufficient time to process the worst case would be to seriously degrade the coder's effectiveness. The time should be increased so that enough time is provided to handle the average case without causing a REP sequence to be initiated.

Had the AUTODIN time delay constraint been larger, a much more effective error correction technique could have been recommended. A discussion of possible means to increase this time delay constraint within the present AUTODIN configuration is presented in the appendix.

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APPENDIX

Increase of the AUTODIN Time Delay Constraint -

This appendix will consider means of increasing the time delay constraint experienced in the AUTODIN system when transmission is in the continuous block mode. Only those methods that can be adapted to the present AUTODIN operation with at most a minor modification will be considered. The particular case of a time delay constraint increase of one line block transmission time is considered. The analysis should be valid for increases of multiple line block transmission times.

Three methods have been identified for possible consideration as follows:

1. Transmit two line blocks and then idle for one line block transmission time.

2. Increase the block size by a factor of two and retain the requirement that the ACK or NACK sequence must be received prior to the transmission of the last data character in the second block.

3. Change the AUTODIN retransmit logic to a "go back three" system, i.e. the transmit terminal will require an ACK or NACK sequence from the first block prior to the transmission of the 83rd character in the third block.

Comparison of each of these methods will be on a throughput basis.

Case I -

Idle for one block time after the transmitter has sent the first line block and 82 characters of the second line block.

The efficiency of this system can be calculated as follows:

$$EFF = \frac{\text{time to send two line blocks}}{\text{time to send two blocks plus idle time}}$$

2 line blocks - 1344 bit times

idle time = one line block = 672 bit times

$$EFF = \frac{1344}{1344+672}$$

$$EFF = 2/3$$

Using the results of the Phase I test, we get the probability of error for a 672 bit block to be .151, or, for every 1000 line blocks transmitted, 151 will be in error and will dictate the retransmission of 302 line blocks, or a block retransmission rate of 2 x .151 = .302.

Information rate = 1 - retransmission rate

$$\text{Information Rate} = \frac{672}{958} = 1. - .302 = .698$$

Throughput = Information Rate x EFF.

= .698 x .667

= .465

Case II -

When the block length is doubled to 1344 bits and the retransmission logic remains the same; i.e. continuous transmission stops if the ACK or NACK sequence is not received prior to the transmission of the 167th character of the second block, a transmission time gain of 84 characters or 672 bit times is achieved.

Since neither the transmit nor the receive terminal is required to idle, the efficiency of this method is equal to 1.

Referring back to our Phase I results, we get the probability of error for a 1344-bit line block to be .206. Since the block size is double, we would only have to transmit 500 line blocks to get the same information between the two terminals as we did in Case 1. The retransmission rate is 2 x .206 or .412.

Information Rate = 1 - retransmission rate = 1 - .412 = .588

Throughput Rate = Inf Rate x Eff

Throughput Rate = .588 x 1

= .588

Case III -

Change the retransmit logic to a "go back three" system. The data transmit terminal will be required to store 3 adjacent line blocks. An ACK or NACK sequence

would be required on the first block before transmitting the 83rd character of the third block. In this system there are always two blocks in transmit rather than the normal one block.

Since there is no idle time, efficiency is equal to one. The error rate for a 672 bit block, as determined from the Phase I data is, again, .151. This time, however, we must retransmit 3 line blocks for each line block received in error. The retransmission rate is therefore 3 x .151 or .453.

Information Rate = 1 - retransmission rate = 1 - .453 = .547

Throughput Rate = Inf Rate x Eff

= .547 x 1 = .547

It is obvious that the method analyzed in Case 1 is not the desired solution. As the block error rate approaches zero the throughput rate approaches .667 as a limit. For the methods analyzed in Case II and Case III, the throughput approaches 1 as a limit when the block error rate approaches zero.

A choice between the Case II and Case III methods is not quite clear. For the data taken in our test the Case II method showed a slight throughput advantage. As the block error rate or the bit error distribution pattern changes, this result would also change.

In general, when a constraint time increase of n blocks is required the Case II technique will have a throughput rate advantage over the Case III method whenever two times the block error rate for the (n x 672) bit block is less than n times the block error rate for a normal size AUTODIN block. This condition will occur if the errors on the channel tend to be clustered in long bursts. As the errors tend to a more random distribution the Case III method will show a throughput advantage.

Modifications required to the AUTODIN terminal to handle the Case II and Case III methods for increasing the AUTODIN time delay constraint would be similar. Within the present system, data is read from drum storage into a high speed memory. From the high speed memory, it is read into the Accumulation and Distribution Unit (ADU). The ADU is used in full duplex operation and contains a transmit and receive section. At the transmit section two line blocks are held in buffer storage until each receives a proper ACK or NACK sequence identified with it. The retransmission logic is as explained earlier. The ADU however, has a capability of storing up to 10 line blocks. This capability is not presently used.

The implementation of the Case II method would require the storage of four 84-character line blocks at the transmitter. Between the transmit and receive ADU's only, the first and second 84-character line blocks would be considered as one 168-character line block. The third and fourth 84-character line blocks would also be considered as

one 168-character line block. Parity checking would still be performed on the 84-character sub-blocks. An error in either of the 84-character sub-blocks would cause the entire 168-character block to be in error. The retransmission logic would be changed such that an ACK or NACK sequence is not expected back until the 82nd character of the fourth sub-block is transmitted. The receive ADU would pass correct data to the data sink in 84 character line blocks. The modification would be completely within the ADU's. The 168 character blocks would be used only between two ADU's in trunk operation. Elsewhere, the normal 84-character blocks would be used.

Case III implementation is somewhat more involved. In this case, three line blocks would be read into the ADU. The retransmit logic would be programmed to expect an ACK or NACK sequence prior to transmission of the 83rd character of the third block. The 84-character line block unit would be maintained throughout the AUTODIN system. Two line blocks would always be in transit. An error in any line block would cause the retransmission of three data blocks. An ACK-3 sequence would have to be developed to retain block synchronization between data terminals. This would entail sacrificing one of the control characters in the American Standard Code for Information Interchange (ASCII) for use as an ACK-3 character. In addition, another bit would have to be used in the tally count word, the internal computer-control word used to service the ADU's, to identify the ACK-3 character.

We would recommend that a modification along the lines discussed in our Case II and Case III analyses be made. The additional time, if used for a forward acting error correction code, would significantly reduce the block error rate. The throughput rate as calculated in Case II and Case III is strongly influenced by the block error rate. A sharp reduction in the block error rate would provide a significant increase in throughput in both the Case II and Case III analyses.

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13 ABSTRACT

The Defense Communications Agency (DCA) sought to determine if the quality of high speed digital data transmitted over long-haul HF radio circuits could be improved by the use of commercially available forward error correction (FEC) devices. The DCA objective was to improve the bit error rate such that HF radio channels could be reliably used as overflow and restoral circuits between Switching Centers within the AUTODIN System. Accordingly a study, analysis and test program was initiated at RADC to satisfy the following requirements defined by DCA.

1. Determine the maximum data rate transmission over HF radio channels within allowable AUTODIN error rates using FEC devices.

2. Determine actual extent of improvement through the use of FEC devices.

3. Analyze FEC operation within the AUTODIN ARQ System.

4. Ascertain modifications for efficient operation of:

AUTODIN ARQ
AUTODIN Procedures
AUTODIN Modems

(See Attached Sheet)

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14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
HF COMMUNICATIONS						
DATA TRANSMISSION						
AUTODIN						
INFORMATION THEORY						
CODING						

5. Provide a procurement specification for DCA use in future equipment purchases.

The study portion of the program resulted in recommendations for the procurement of three representative, commercially available coding equipments and a fully documented test plan for the evaluation of these equipments on a transcontinental HF radio circuit.

A three phase test program was carried out during the months of February through August 1967. A full duplex HF radio path was established between McClellan AFB in Sacramento, California, and Griffiss AFB, Rome, New York. The AUTODIN Switches at McClellan AFB and at Hancock Field, Syracuse, New York were connected to the radio path by data quality phone lines and microwave links. In one of the test phases AUTODIN traffic was passed between these two terminals in full duplex operation for a period of five weeks. Circuit quality was evaluated in terms of block error rate and data throughput rate for uncoded data and for data protected by each of the FEC devices tested. The other two test phases were concerned with deriving the fine grain bit error pattern statistics of the channel and an analysis of the operation of the AUTODIN data switches. The latter test phase utilized the DICOSE facility at RADC to simulate AUTODIN switch operation in order to obtain data that was not available in normal AUTODIN switch operation.

Over 375 hours of data taken at trunk data rates of 1200 bits per second were analyzed. Performance characteristics for each of the error correction devices tested as well as the uncoded channel operation were provided to DCA. A recommendation incorporating an error correction device into the AUTODIN System for use on HF radio backup circuits was made. The recommendation included a complete procurement specification. In addition, recommendations were made concerning modem operation and the interface of the AUTODIN switch with the HF radio sites.